User's Guide

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For Safety Information, Warranties, and Regulatory Information, see the pages at the end of this manual.

HP E2447AA/AB Analysis Probe for Motorola MC68000/010

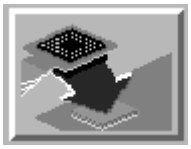
The HP E2447AA/AB Analysis Probe — At a Glance

The HP E2447AA and HP E2447AB Analysis Probes provide a complete interface for state or timing analysis between any of the supported microprocessors listed below and HP logic analyzers. The supported logic analyzers are listed in chapter 1.

Supported Microprocessors

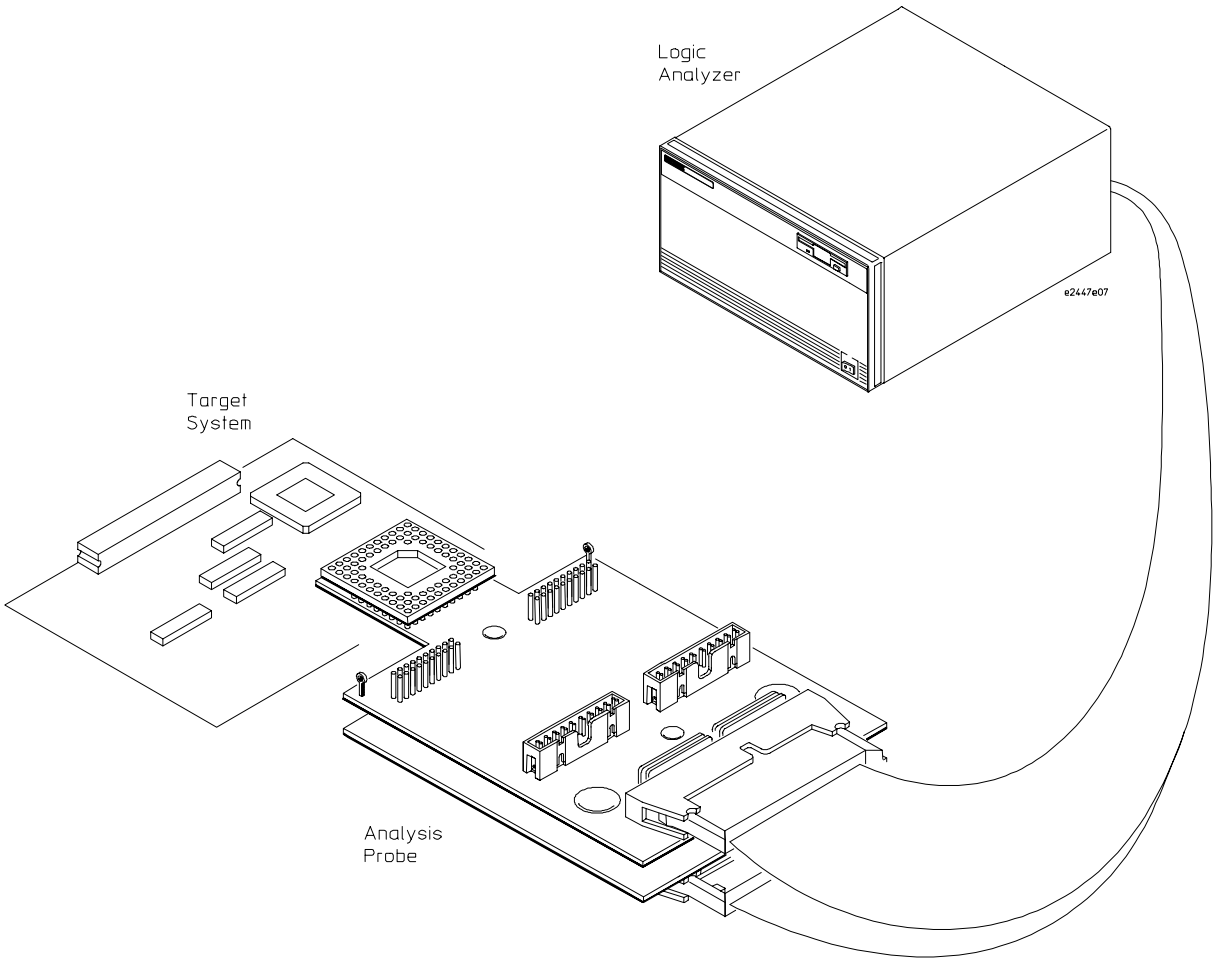
Microprocessor	Package	Ordering Information
MC68000	68-pin PGA	E2447AA
MC68HC000	68-pin PGA	E2447AA
MC68010	68-pin PGA	E2447AA
MC68000, MC68010, MC68HC000	DIP	E2447AA and ET DIP-to-PGA (68-pin) adapter
MC68EC000	69-pin PLCC	E2447AB

The analysis probe provides the physical connection between the target microprocessor and the logic analyzer. The configuration software on the enclosed disks set up the logic analyzer for compatibility with the analysis probe. The inverse assembler lets you obtain displays of the 68000/010 data bus in 68000/010 assembly language mnemonics.



If you are using the analysis probe with the HP 16600 or HP 16700 series logic analysis systems, you only need this manual as a reference. The HP 16600 and 16700 series contain a Setup Assistant, which guides you through the connection and configuration process using on screen dialog windows. For an overview of Setup Assistant, refer to Chapter 1, "Setup Assistant."

For more information on the logic analyzers or microprocessor, refer to the appropriate reference manuals for those products.

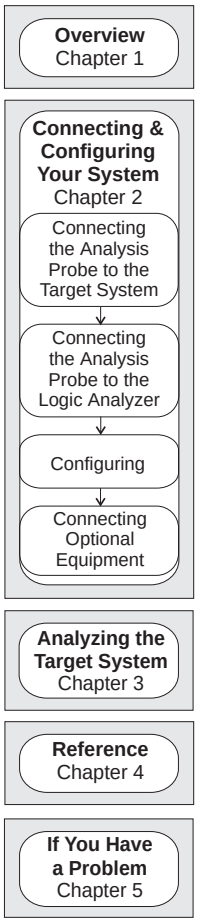


Analyzing a Target System with the HP E2447AA/AB Analysis Probe

In This Book

This book is the User's Guide for the HP E2447AA/AB Analysis Probes. It assumes that you have a working knowledge of the logic analyzer used and the microprocessor being analyzed.

This user's guide is organized into the following chapters:



Chapter 1 contains overview information, including a list of required equipment.

Chapter 2 explains how to connect the logic analyzer to your target system through the analysis probe, and how to configure the analysis probe and logic analyzer to interpret target system activity. The last section in this chapter shows you how to hook up optional equipment to obtain additional functionality.

HP 16600 and HP 16700 Series Logic Analysis Systems

If you are using the analysis probe with HP 16600 or HP 16700 series logic analysis systems, you only need this manual as a reference for obtaining and interpreting data. The HP 16600 and HP 16700 contain a Setup Assistant, which guides you through the connection and configuration process using on screen dialog windows. For an overview of Setup Assistant, refer to chapter 1, "Setup Assistant."

Chapter 3 provides information on analyzing the supported microprocessors.

Chapter 4 contains reference information on the analysis probe.

Chapter 5 contains troubleshooting information.

Contents

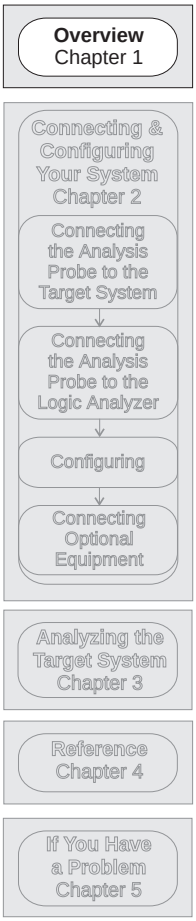
1

Overview

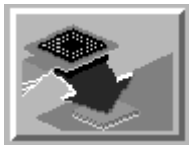
Overview

This chapter describes:

- Setup Assistant
- Logic analyzers supported
- Logic analyzer software version requirements
- Equipment used with the analysis probe
- Equipment supplied
- Minimum equipment required
- Additional equipment supported



Setup Assistant



Setup Assistant is an online tool for connecting and configuring your logic analysis system for microprocessor and bus analysis. Setup Assistant is available on the HP 16600 and HP 16700 series logic analysis systems. You can use Setup Assistant in place of the connection and configuration procedures provided in chapter 2.

This menu-driven tool will guide you through the connection procedures for connecting the logic analyzer to an analysis probe, an emulation module, or other supported equipment. It will also guide you through connecting an analysis probe to the target system.

Access Setup Assistant by clicking its icon in the Logic Analysis System window. The on-screen dialog prompts you to choose the type of measurements you want to make, the type of target system, and the associated products that you want to set up.

If you ordered this product with your HP 16600/700 logic analysis system, the logic analysis system has the latest software installed, including support for this product. If you received this product after you received your logic analysis system, this product might not be listed under supported products. In that case, you need to install the M68000 Processor Support Package. Use the procedure on the CD-ROM jacket to install the M68000 Processor Support Package.

Logic Analyzers Supported

The table below lists the logic analyzers supported by the HP E2447AA/AB analysis probe. Logic analyzer software version requirements are shown on the following page.

The HP E2447AA/AB requires three logic analyzer pods (51 channels) for inverse assembly. The analysis probe contains one additional state pod, and three additional timing pods that you can monitor.

Logic Analyzers Supported

Logic Analyzer	Channel Count	State Speed	Timing Speed	Memory Depth
16600A	204	100 MHz	125 MHz	64 k states
16601A	136	100 MHz	125 MHz	64 k states
16602A	102	100 MHz	125 MHz	64 k states
16603A	68	100 MHz	125 MHz	64 k states
16550A (one card)	102/card	100 MHz	250 MHz	4 k states
16554A (one card)	68/card	70 MHz	125 MHz	512 k states
16555A (one card)	68/card	110 MHz	250 MHz	1 M states
16555D (one card)	68/card	110 MHz	250 MHz	2 M states
16556A (one card)	68/card	100 MHz	200 MHz	1 M states
16556D (one card)	68/card	100 MHz	200 MHz	2 M states
1660A/AS/C/CS/CP	136	100 MHz	250 MHz	4 k states
1661A/AS/C/CS/CP	102	100 MHz	250 MHz	4 k states
1662A/AS/C/CS/CP	68	100 MHz	250 MHz	4 k states
1670A	136	70 MHz	125 MHz	64 k or .5 M states
1670D	136	100 MHz	125 MHz	64 k or 1 M states
1671A	102	70 MHz	125 MHz	64 k or .5 M
1671D	102	100 MHz	125 MHz	64 k or 1 M
1672A	68	70 MHz	125 MHz	64 k or .5 M
1672D	68	100 MHz	125 MHz	64 k or 1 M

Logic analyzer software version requirements

The logic analyzers must have software with a version number greater than or equal to those listed below to make a measurement with the HP E2447AA/AB. You can obtain the latest software at the following web site:
www.hp.com/go/logicanalyzer

If your software version is older than those below, load new system software with the listed version numbers or higher before loading the HP E2447AA/AB software.

Logic Analyzer Software Version Requirements

Logic Analyzer	Minimum Logic Analyzer Software Version for use with HP E2447AA/AB
HP 16600 Series	The latest HP 16600 logic analyzer software version is on the CD-ROM shipped with this product.
HP 1660A/AS Series	A.03.01
HP 1660C/CS/CP Series	A.02.01
HP 1670A/D Series	A.02.01
Mainframes*	
HP 16700 Series	The latest HP 16700 logic analyzer software version is on the CD-ROM shipped with this product.
HP 16500C Mainframe	A.01.05
HP 16500B Mainframe	A.03.14

* The mainframes are used with the HP 16550 and HP 16554/55/56 logic analyzer modules.

Equipment Used with the Analysis Probe

This section lists equipment used with the analysis probe. This information is organized under the following titles: equipment supplied, minimum equipment required, and additional equipment supported

Equipment supplied

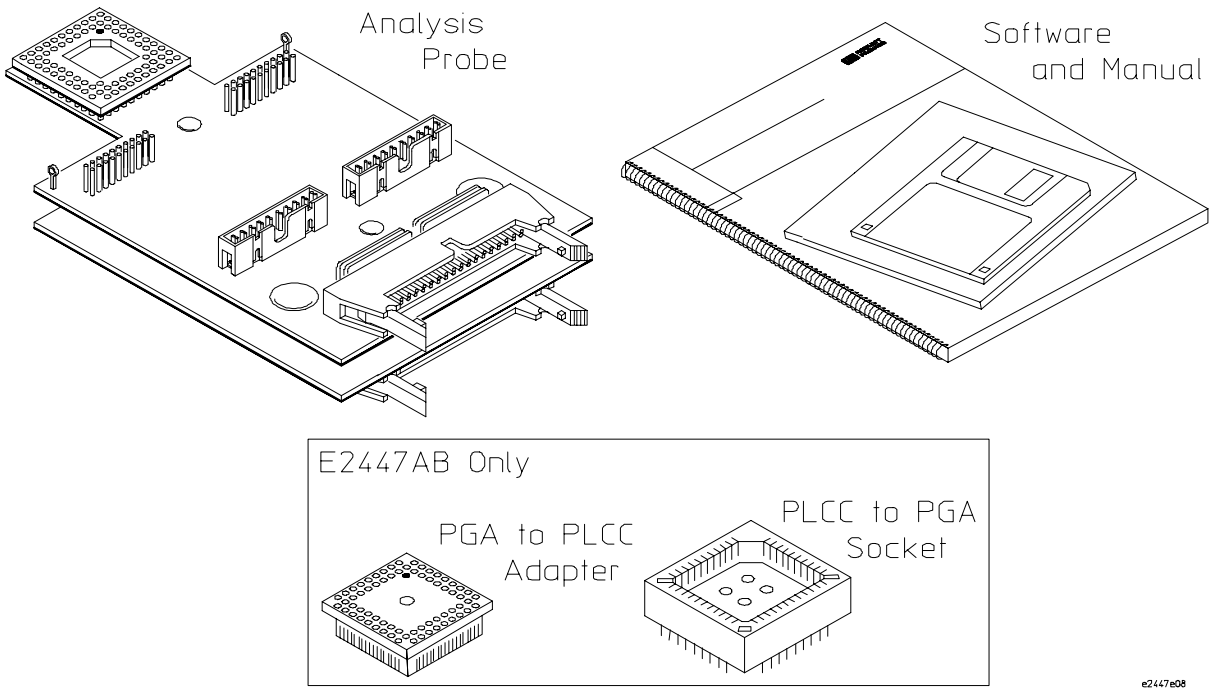
The equipment supplied with the analysis probe is shown in the illustration on the next page. It is listed below:

E2447AA

- The HP E2447AA 68-pin analysis probe, which includes the analysis probe circuit card and cables.
- Logic analyzer configuration files and inverse assembler software on a 3.5-inch disk.
- Logic analyzer configuration files and inverse assembler software on a CD-ROM.
- This User's Guide.

E2447AB

- The HP E2447AB 69-pin analysis probe, which includes the analysis probe circuit card and cables.
- One PGA to PLCC Adapter, HP part number E2434-63201.
- One PLCC to PGA Socket, HP part number 1200-1722.
- Logic analyzer configuration files and inverse assembler software on a 3.5-inch disk.
- Logic analyzer configuration files and inverse assembler software on a CD-ROM.
- This User's Guide.



Equipment Supplied with the HP E2447AA/AB

Minimum equipment required

For state and timing analysis of a 68000/010 target system, you need all of the following items.

- The HP E2447AA or HP E2447AB Analysis Probe.
- For PLCC target systems, the two adapters that come with the HP E2447AB.
- For PLCC target systems, a socketed PLCC target system. Surface-mounted PLCC systems will not work.
- For DIP target systems, a DIP-to-PGA adapter from Emulation Technology.
- For Timing analysis, either the General Purpose Probes shipped with your logic analyzer or three 100 kOhm Termination Adapters (HP part number 01650-63203).
- One of the logic analyzers listed on page 1-4. The logic analyzer software version requirements are listed on page 1-5.

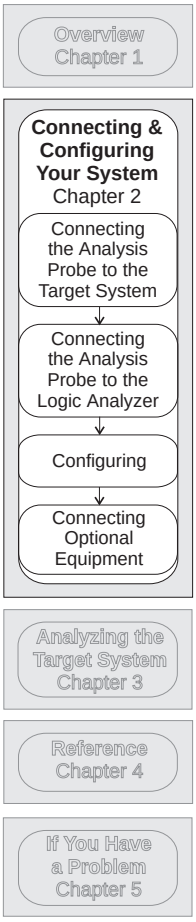
Additional equipment supported

The HP E2447AA/AB does not support any additional equipment.

2

Connecting and Configuring Your System

Connecting and Configuring Your System



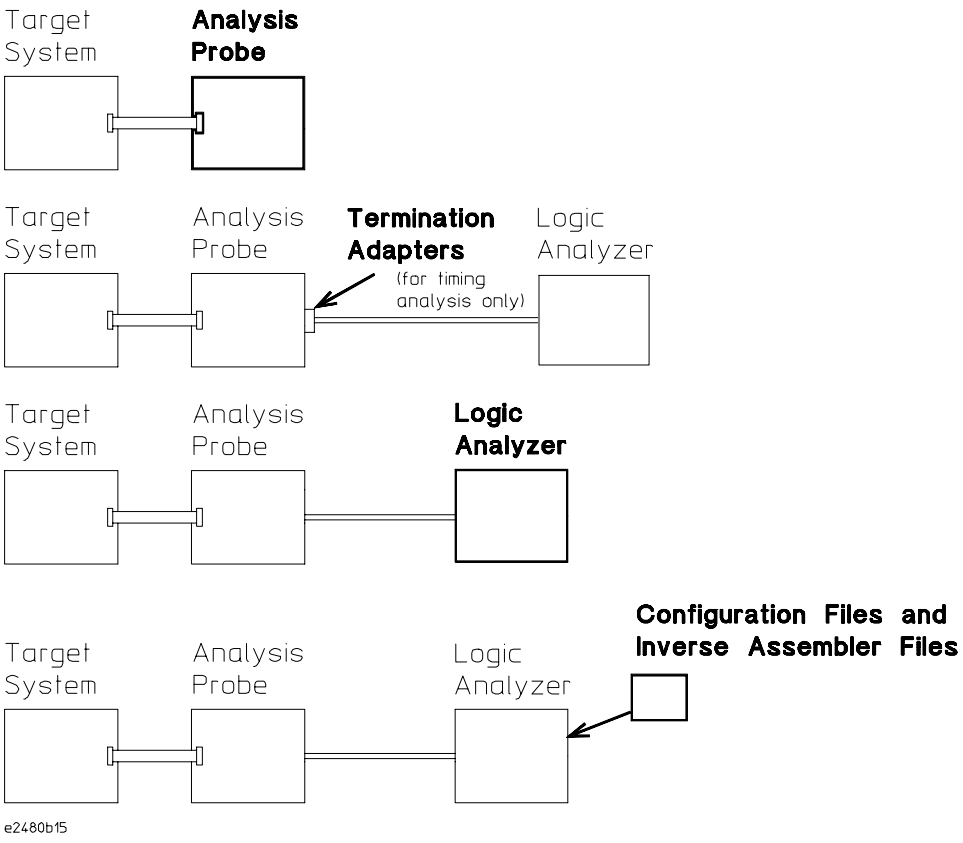
This chapter shows you how to connect the logic analyzer to the target system through the analysis probe.

If you are connecting to an HP 16600 or HP 16700 series logic analysis system, follow the instructions given on screen in the Setup Assistant for connecting and configuring your system. Use this manual for additional information, if desired. Refer to chapter 1 for a description of Setup Assistant.

If you are not using the Setup Assistant, follow the instructions given in this chapter. This chapter is divided into the following sections; the order shown here is the recommended order for performing these tasks:

- Read the power on/power off sequence
- Connect the analysis probe to the target system
- Connect the analysis probe to the logic analyzer
- Configure the logic analyzer
- Connect optional equipment

Read the power on/power off sequence.



Connection Sequence

Power-on/Power-off Sequence

Listed below are the sequences for powering on and off a fully connected system. Simply stated, your target system is always the last to be powered on, and the first to be powered off.

To power on HP 16600 and HP 16700 series logic analysis systems

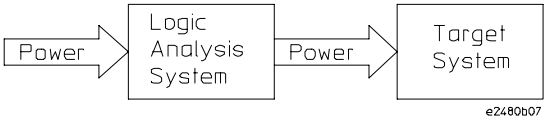
Ensure the target system is powered off.

1. Turn on the logic analyzer. The Setup Assistant will guide you through the process of connecting and configuring the analysis probe.
2. When the analysis probe is connected to the target system and logic analyzer, and everything is configured, turn on your target system.

To power on all other logic analyzers

With all components connected, power on your system in the following order:

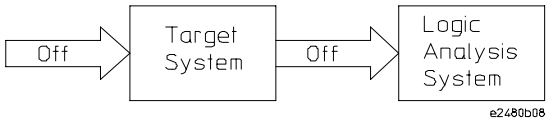
1. Logic analysis system.
2. Your target system.



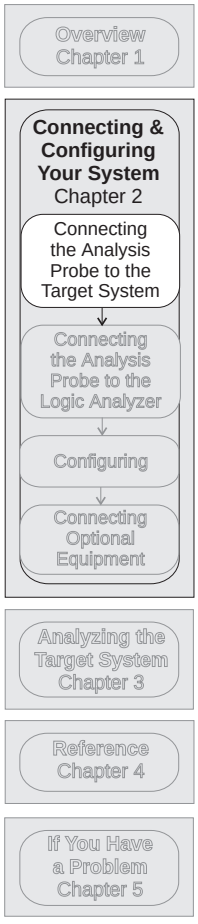
To power off

Turn off power to your system in the following order:

1. Turn off your target system.
2. Turn off your logic analysis system.



Connecting the Analysis Probe to the Target System



This section explains how to connect the HP E2447AA/AB Analysis Probe to the target system. Connecting the analysis probe to the target system consists of the following tasks:

- For PGA target systems, connect the analysis probe directly to the target system.

  Refer to "To connect to a PGA target system."
- For PLCC target systems, connect the adapter socket to the target system.

  Refer to "To connect to a PLCC target system."
- For PLCC target systems, connect the analysis probe to the adapter.

The remainder of this section describes these general tasks in more detail.

Protect Your Equipment

The analysis probe socket assembly pins are covered for shipment with a conductive foam wafer or conductive plastic pin protector. This is done to protect the delicate gold-plated pins from damage due to impact. When you are not using the analysis probe, protect the socket assembly pins from damage by covering them with the pin protector.

To connect to a PGA target system

CAUTION

Equipment Damage. To prevent equipment damage, remove power from the target system and make sure no logic analyzer cables are connected to the analysis probe.

1. Turn off the target system and disconnect all logic analyzer cables from the analysis probe.
2. Remove the microprocessor from its socket on the target system and store it in a protected environment.
3. Prior to inserting the analysis probe PGA connector in the target system socket, note the position of pin 1 on the analysis probe connector and the target system socket (refer to the figure on next page).
4. Carefully align the analysis probe connector with the socket on the target system so that all pins are making contact.

CAUTION

Serious damage to the target system or analysis probe can result from incorrect connection. Ensure that pin 1 on the analysis probe and the target system are aligned, and that all pins are making contact.

5. Plug the analysis probe connector into the microprocessor socket on the target system.

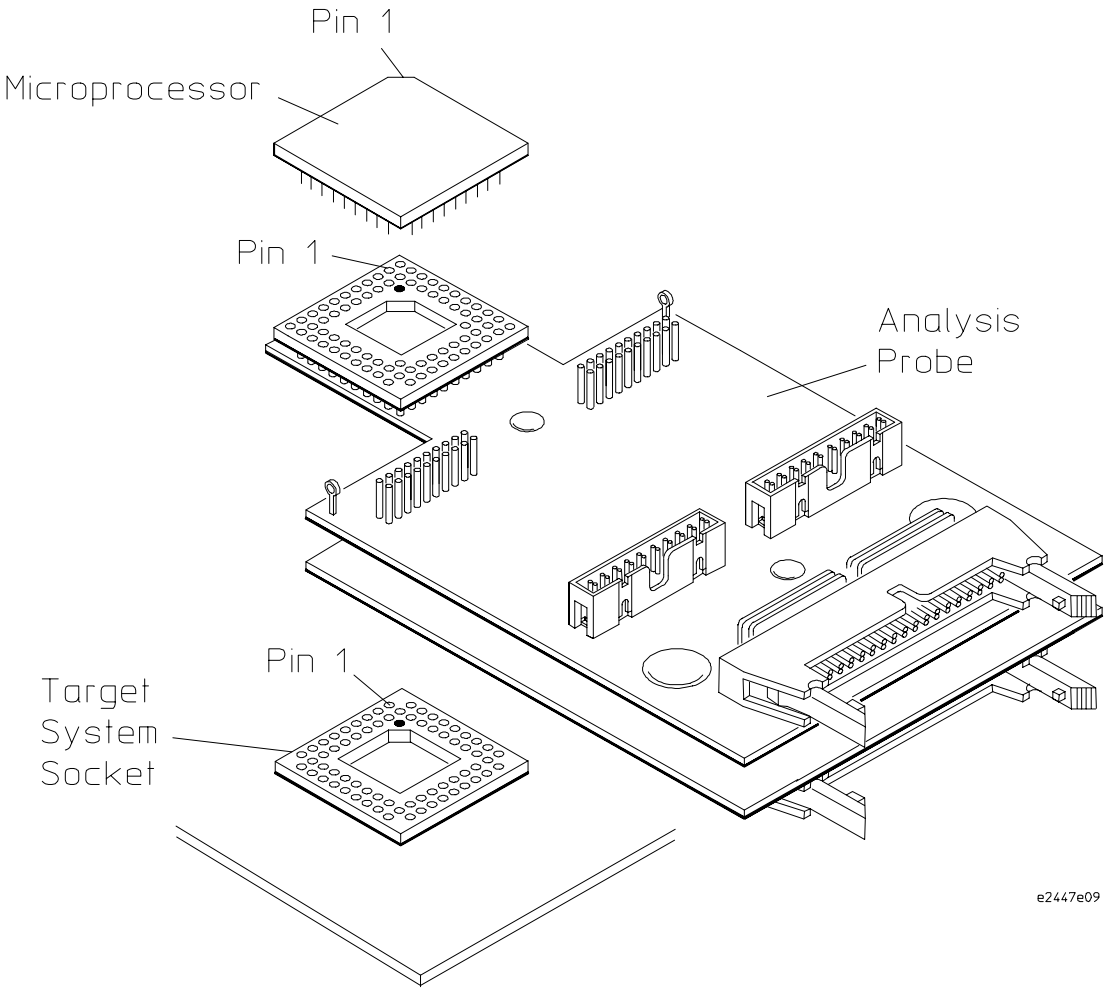
   If the analysis probe circuit board interferes with components of the target system or if a higher profile is required, insert additional plastic pin protectors. You can order plastic pin protectors from Hewlett-Packard using the part number 1200-1721. However, any 68-pin PGA IC socket with a 68000/010 footprint and gold-plated pins can be used.

6. Plug the microprocessor into the socket of the analysis probe board.

   The socket on the analysis probe board is designed with low-insertion-force pins to allow you to install or remove the microprocessor with a minimum amount of force.

CAUTION

Do not use sharp objects or excessive force when removing a microprocessor or socket from the analysis probe board. Traces on the analysis probe board may be damaged.



Pin 1 Location

To connect to a PLCC target system

The PLCC adapters provide a connection between the analysis probe and the 68-pin PLCC microprocessor. The PLCC adapter attaches to the target system PLCC socket. The analysis probe PGA pins connect to the adapter socket. The adapters consist of the following:

- PLCC adapter
- PLCC socket

Use the following procedure to connect to a PLCC target system.

1 Using a PLCC extractor tool, remove the microprocessor from the PLCC socket on the target system.

CAUTION Be careful not to damage the PLCC socket or the microprocessor when removing the microprocessor from the target system.

2 Store the microprocessor in a protected environment.

CAUTION Serious damage to the target system or analysis probe can result from incorrect connection. Ensure that pin 1 on the analysis probe, PLCC adapter, and the target system are aligned, and that all pins are making contact.

3 Noting the position of pin 1, place the PLCC adapter in the microprocessor socket of the target system (refer to the figure on next page).

4 Plug the analysis probe connector into the PLCC adapter.

If the analysis probe circuit board interferes with components of the target system or if a higher profile is required, insert additional plastic pin protectors. You can order plastic pin protectors from Hewlett-Packard using the part number 1200-1723.

5 Using one of the following methods, install the microprocessor.

a If a PGA-style 68010 microprocessor is available, note the location of pin 1 on the microprocessor and the analysis probe socket and insert the PGA microprocessor in the socket on top of the analysis probe.

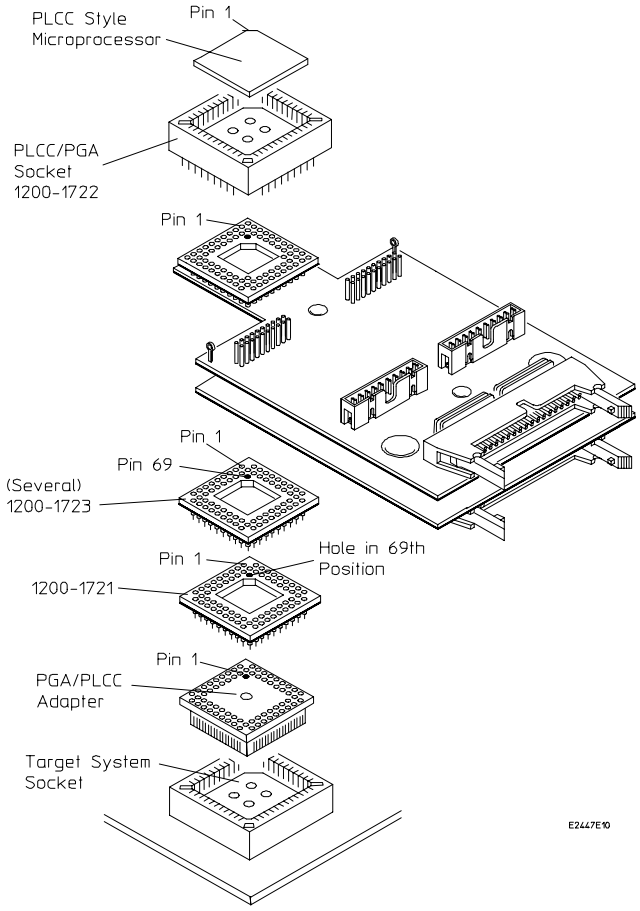
b If a PGA microprocessor is not available, note the location of pin 1 on the PLCC socket and the analysis probe socket, and install the PLCC socket on the analysis probe. Plug the PLCC microprocessor into the PLCC socket.

CAUTION

To prevent pin damage and ensure proper connection, make sure the pins are aligned and seated correctly in the socket.

CAUTION

The weight of the analysis probe can apply enough force to disconnect the PGA to PLCC Adapter. To prevent accidental disconnections, support the analysis probe in a stable position.



Installing the PLCC Adapter and PLCC Socket

The PLCC socket adds additional capacitance to the circuit, but should not affect the performance of the microprocessor.

Connecting the Analysis Probe to the Logic Analyzer

Overview
Chapter 1

Connecting & Configuring Your System
Chapter 2
Connecting the Analysis Probe to the Target System
Connecting the Analysis Probe to the Logic Analyzer
Configuring
Connecting Optional Equipment

Analyzing the Target System
Chapter 3

Reference
Chapter 4

If You Have a Problem
Chapter 5

The following sections show the connections between the logic analyzer pod cables and the analysis probe cables. Use the appropriate section for your logic analyzer. The configuration file names for each logic analyzer are located at the bottom of the connection diagrams.

A minimum of three analysis probe pods are required for inverse assembly. A fourth pod contains additional signals you can monitor. The illustration on the following page shows the analysis probe pod locations.

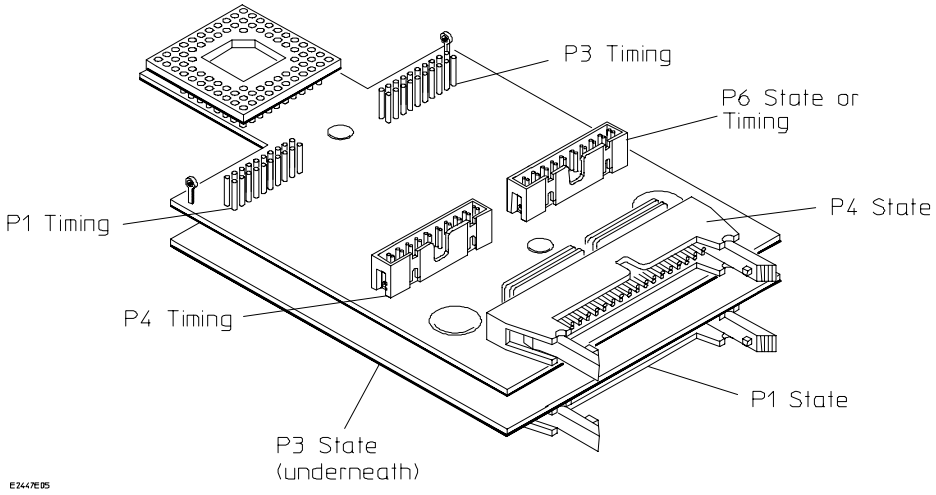
For State analysis, use State connectors P1, P3, and P4. For Timing analysis, use either General Purpose probes or termination adapters, and connect to Timing connectors P1, P3, and P4. P6 is optional for state and timing.

This section shows connection diagrams for connecting the analysis probe to the logic analyzers listed below:

- HP 16600A logic analysis system
- HP 16601A logic analysis system
- HP 16602A logic analysis system
- HP 16603A logic analysis system
- HP 16550A logic analyzer (one card)
- HP 16554/55/56 logic analyzers (one card)
- HP 1660A/AS/C/CS/CP logic analyzers
- HP 1661A/AS/C/CS/CP logic analyzers
- HP 1662A/AS/C/CS/CP logic analyzers
- HP 1670A/D logic analyzers
- HP 1671A/D logic analyzers
- HP 1672A/D logic analyzers

Analysis probe pod locations

The illustration below shows the pod locations on the analysis probe.



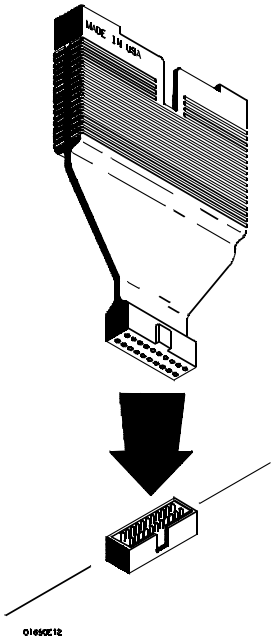
HP E2447AA/AB Analysis Probe Pod Locations

To connect the termination adapters

The logic analyzer probes must be properly terminated for the logic analyzer to operate correctly. On the analysis probe, there are seven connectors. P1, P3, and P4 have both terminated and nonterminated connectors, while P6 only has a nonterminated connector. You can probe P6 (and the nonterminated P1, P3, and P4 connectors) with the General Purpose Probes shipped with your logic analyzer or by using 100 kOhm Termination Adapters (HP part number 01650-63203).

To connect the termination adapters for Timing analysis:

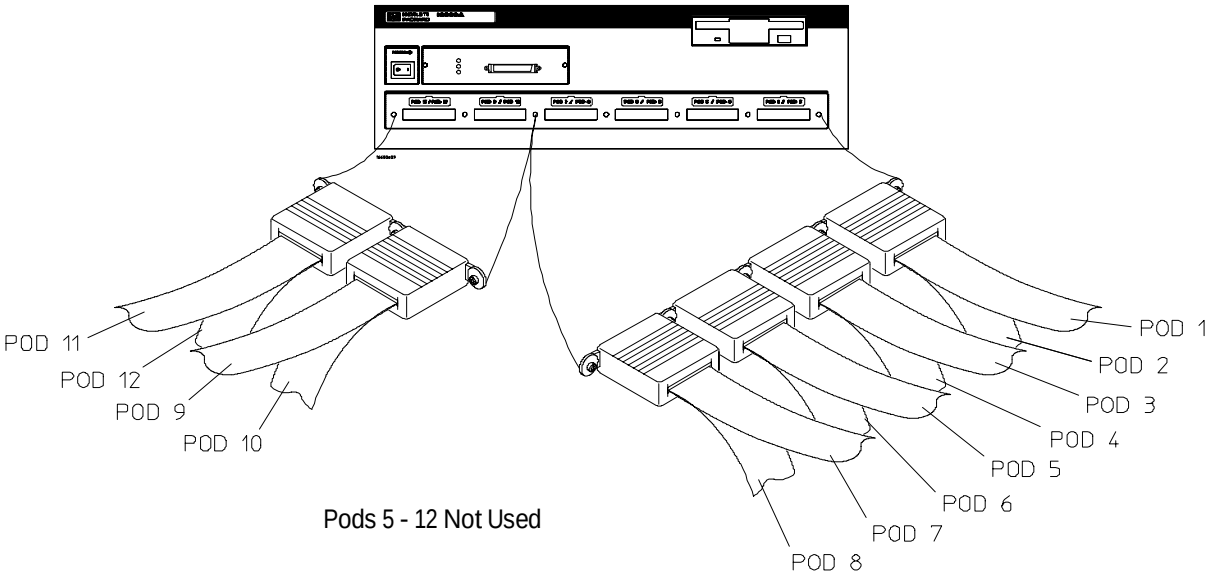
- Connect the female end of the termination adapter to the analysis probe.
- Align the key on the male end of the termination adapter with the slot on the connector of the appropriate logic analyzer cables. Push the termination adapter into the connector.



Connecting the Termination Adapters for Timing Analysis

To connect to the HP 16600A logic analysis system

Use the figure and table below to connect the analysis probe to the HP 16600A logic analysis system.



HP 16600	Pods 5 - 12	Pod 4	Pod 3	Pod 2	Pod 1
HP E2447AA/AB Connector	not used	P4 ** ADDR/STAT clk ↑	P3 ADDR	P6 *	P1 DATA

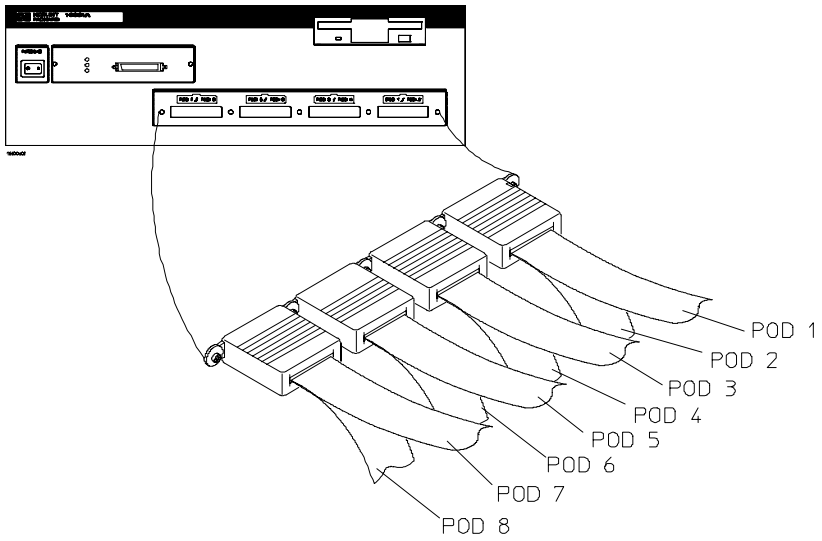
* P6 on the analysis probe is not required for inverse assembly. You can connect it to logic analyzer Pod 2, or leave it unconnected. Use GP Probes or termination adapters to monitor these signals.

** For inverse assembly, only the terminated (2 x 20-pin wide) P4 connector can be used. For timing analysis, use the unterminated 2x10 pin P4 connector.

Configuration File
Use configuration files F68000 or F68010 with the HP E2447AA, or FEC000 with the HP E2447AA for the HP 16600 logic analysis system.

To connect to the HP 16601A logic analysis system

Use the figure and table below to connect the analysis probe to the HP 16601A logic analysis system.



HP 16601	Pods 5 - 8	Pod 4	Pod 3	Pod 2	Pod 1
HP E2447AA/AB Connector	not used	P4 ** ADDR/STAT clk ↑	P3 ADDR	P6 *	P1 DATA

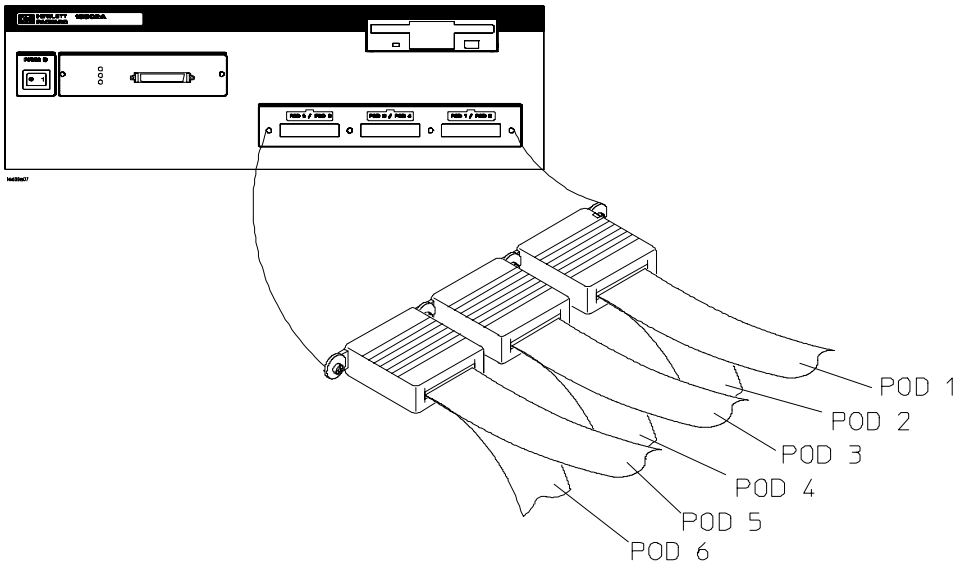
* P6 on the analysis probe is not required for inverse assembly. You can connect it to logic analyzer Pod 2, or leave it unconnected. Use GP Probes or termination adapters to monitor these signals.

** For inverse assembly, only the terminated (2 x 20-pin wide) P4 connector can be used. For timing analysis, use the unterminated 2x10 pin P4 connector.

Configuration File
Use configuration files F68000 or F68010 with the HP E2447AA, or FEC000 with the HP E2447AA for the HP 16601 logic analysis system.

To connect to the HP 16602A logic analysis system

Use the figure and table below to connect the analysis probe to the HP 16602A logic analysis system.



HP 16602	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP E2447AA/AB Connector	not used	not used	P4 ** ADDR/STAT clk ↑	P3 ADDR	P6 *	P1 DATA

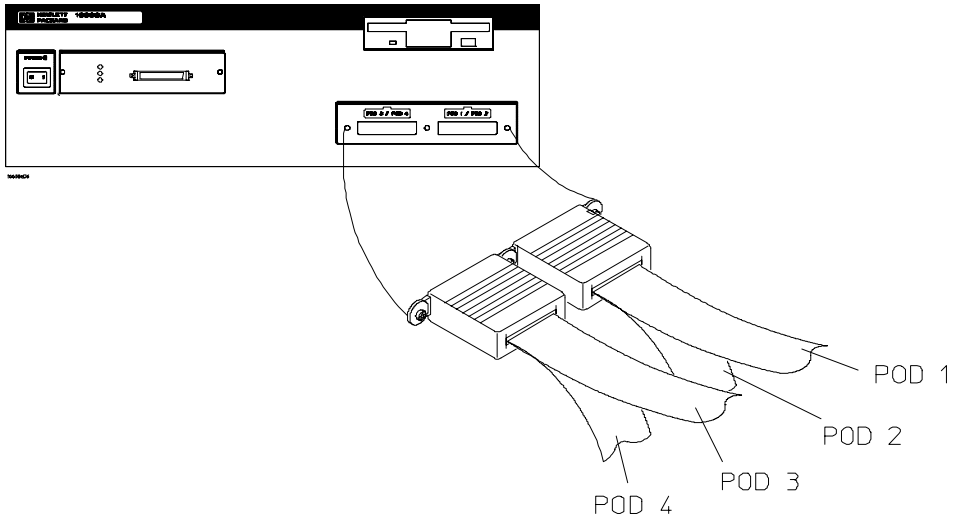
* P6 on the analysis probe is not required for inverse assembly. You can connect it to logic analyzer Pod 2, or leave it unconnected. Use GP Probes or termination adapters to monitor these signals.

** For inverse assembly, only the terminated (2 x 20-pin wide) P4 connector can be used. For timing analysis, use the unterminated 2x10 pin P4 connector.

Configuration File
Use configuration files F68000 or F68010 with the HP E2447AA, or FEC000 with the HP E2447AA for the HP 16602 logic analysis system.

To connect to the HP 16603A logic analysis system

Use the figure and table below to connect the analysis probe to the HP 16603A logic analysis system.



HP 16603	Pod 4	Pod 3	Pod 2	Pod 1
HP E2447AA/AB Connector	P4 ** ADDR/STAT clk ↑	P3 ADDR	P6 *	P1 DATA

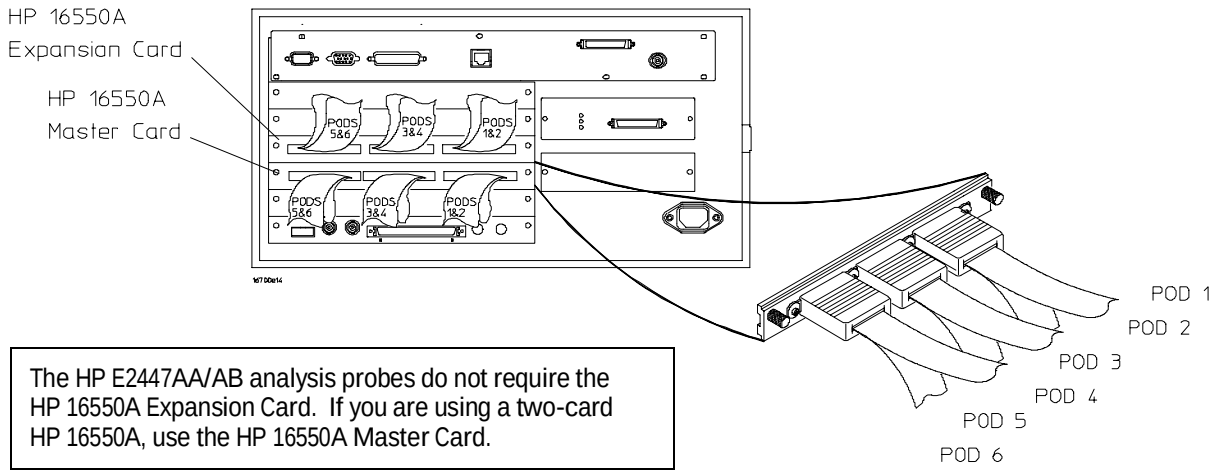
* P6 on the analysis probe is not required for inverse assembly. You can connect it to logic analyzer Pod 2, or leave it unconnected. Use GP Probes or termination adapters to monitor these signals.

** For inverse assembly, only the terminated (2 x 20-pin wide) P4 connector can be used. For timing analysis, use the unterminated 2x10 pin P4 connector.

Configuration File
Use configuration files F68000 or F68010 with the HP E2447AA, or FEC000 with the HP E2447AA for the HP 16603 logic analysis system.

To connect to the HP 16550A logic analyzer

Use the figure and table below to connect the analysis probe to the HP 16550A logic analyzer.



The HP E2447AA/AB analysis probes do not require the HP 16550A Expansion Card. If you are using a two-card HP 16550A, use the HP 16550A Master Card.

HP 16550A Master Card	Master Card Pod 6	Master Card Pod 5	Master Card Pod 4	Master Card Pod 3	Master Card Pod 2	Master Card Pod 1
HP E2447AA/AB Connector	not used	not used	P4 ** ADDR/STAT clk ↑	P3 ADDR	P6 *	P1 DATA

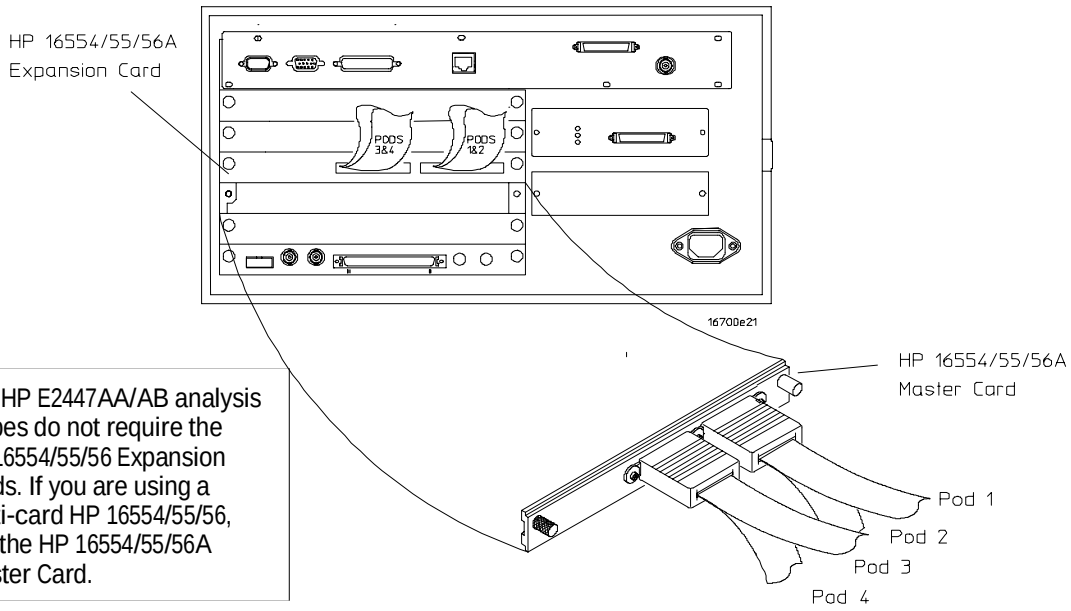
* P6 on the analysis probe is not required for inverse assembly. You can connect it to logic analyzer Pod 2, or leave it unconnected. Use GP Probes or termination adapters to monitor these signals.

** For inverse assembly, only the terminated (2 x 20-pin wide) P4 connector can be used. For timing analysis, use the unterminated 2x10 pin P4 connector.

Configuration File
Use configuration files F68000 or F68010 with the HP E2447AA, or FEC000 with the HP E2447AA for the HP 16550A logic analyzer.

To connect to the HP 16554/55/56 logic analyzers

Use the figure and table below to connect the analysis probe to the HP 16554A/55A/56A and HP 16555D/56D logic analyzers.



The HP E2447AA/AB analysis probes do not require the HP 16554/55/56 Expansion Cards. If you are using a multi-card HP 16554/55/56, use the HP 16554/55/56A Master Card.

HP 16554/55/56 Master Card	Master Card Pod 4	Master Card Pod 3	Master Card Pod 2	Master Card Pod 1
HP E2447AA/AB Connector	P6 *	P1 DATA	P4 ** ADDR/STAT clk ↑	P3 ADDR

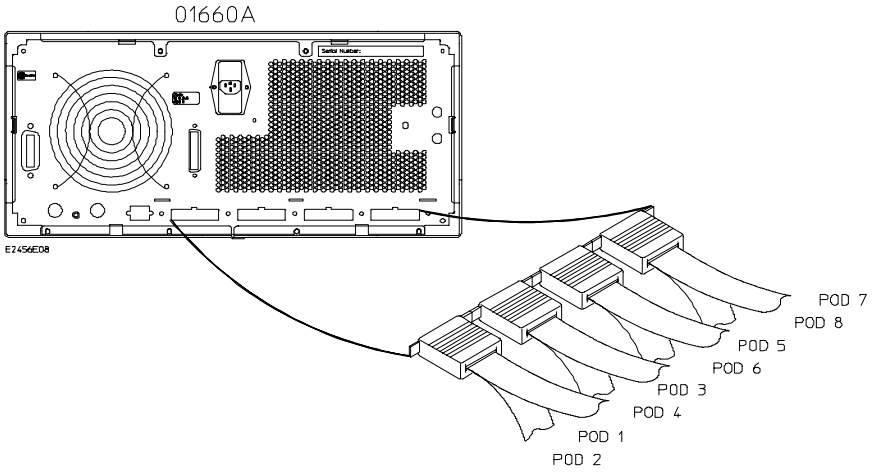
* P6 on the analysis probe is not required for inverse assembly. You can connect it to logic analyzer Pod 2, or leave it unconnected. Use GP Probes or termination adapters to monitor these signals.

** For inverse assembly, only the terminated (2 x 20-pin wide) P4 connector can be used. For timing analysis, use the unterminated 2x10 pin P4 connector.

Configuration File
Use configuration files F68000 or F68010 with the HP E2447AA, or FEC000 with the HP E2447AA for the HP 16554/55/56 logic analyzers.

To connect to the HP 1660A/AS/C/CS/CP logic analyzers

Use the figure and table below to connect the analysis probe to the HP 1660A/C logic analyzers.



HP 1660A/C	Pod 1	Pod 2	Pod 3	Pod 4	Pods 5 - 8
HP E2447AA/AB Connector	P1 DATA	P6 *	P3 ADDR	P4 ** ADDR/STAT clk ↑	not used

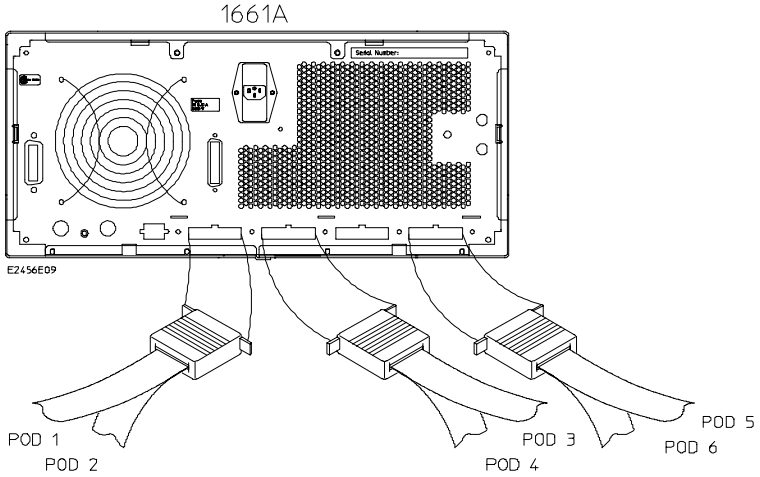
* P6 on the analysis probe is not required for inverse assembly. You can connect it to logic analyzer Pod 2, or leave it unconnected. Use GP Probes or termination adapters to monitor these signals.

** For inverse assembly, only the terminated (2 x 20-pin wide) P4 connector can be used. For timing analysis, use the unterminated 2x10 pin P4 connector.

Configuration File
Use configuration files F68000 or F68010 with the HP E2447AA, or FEC000 with the HP E2447AA for the HP 1660A/AS/C/CS/CP logic analyzers.

To connect to the HP 1661A/AS/C/CS/CP logic analyzers

Use the figure and table below to connect the analysis probe to the HP 1661A/C logic analyzers.



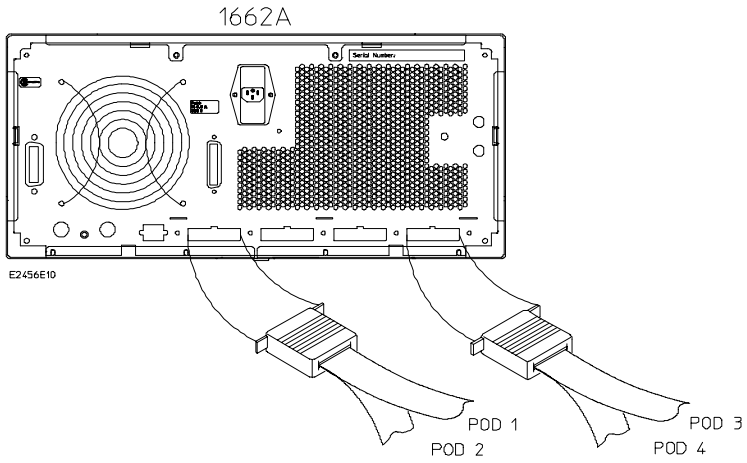
HP 1661A/C	Pod 1	Pod 2	Pod 3	Pod 4	Pod 5	Pod 6
HP E2447AA/AB Connector	P1 DATA	P6 *	P3 ADDR	P4 ** ADDR/STAT clk ↑	not used	not used

* P6 on the analysis probe is not required for inverse assembly. You can connect it to logic analyzer Pod 2, or leave it unconnected. Use GP Probes or termination adapters to monitor these signals.
** For inverse assembly, only the terminated (2 x 20-pin wide) P4 connector can be used. For timing analysis, use the unterminated 2x10 pin P4 connector.

Configuration File
Use configuration files F68000 or F68010 with the HP E2447AA, or FEC000 with the HP E2447AA for the HP 1661A/AS/C/CS/CP logic analyzers.

To connect to the HP 1662A/AS/C/CS/CP logic analyzers

Use the figure and table below to connect the analysis probe to the HP 1662A/C logic analyzers.



HP 1662A/C	Pod 1	Pod 2	Pod 3	Pod 4
HP E2447AA/AB Connector	P1 DATA	P6 *	P3 ADDR	P4 ** ADDR/STAT clk ↑

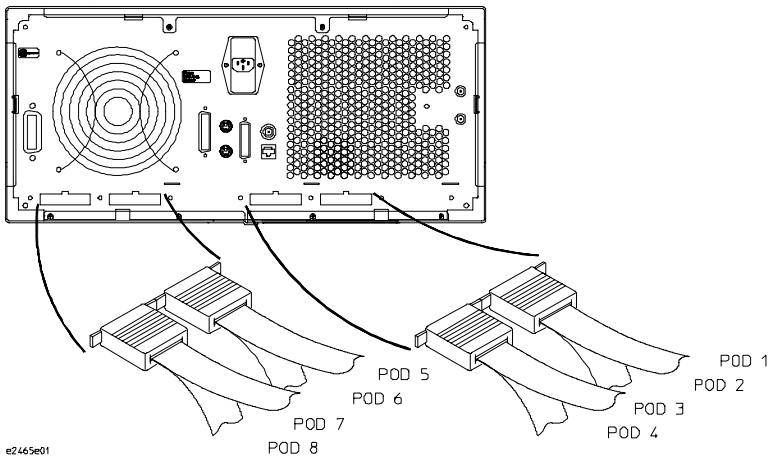
* P6 on the analysis probe is not required for inverse assembly. You can connect it to logic analyzer Pod 2, or leave it unconnected. Use GP Probes or termination adapters to monitor these signals.

** For inverse assembly, only the terminated (2 x 20-pin wide) P4 connector can be used. For timing analysis, use the unterminated 2x10 pin P4 connector.

Configuration File
Use configuration files F68000 or F68010 with the HP E2447AA, or FEC000 with the HP E2447AA for the HP 1662A/AS/C/CS/CP logic analyzers.

To connect to the HP 1670A/D logic analyzer

Use the figure and table below to connect the analysis probe to the HP 1670A/D logic analyzers.



HP 1670A/D	Pods 5 - 8	Pod 4	Pod 3	Pod 2	Pod 1
HP E2447AA/AB Connector	not used	P6 *	P1 DATA	P4 ** ADDR/STAT clk ↑	P3 ADDR

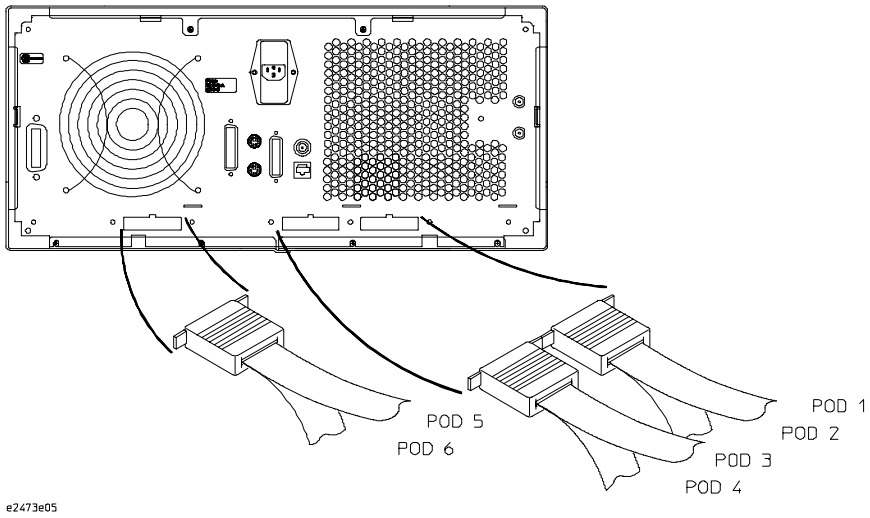
* P6 on the analysis probe is not required for inverse assembly. You can connect it to logic analyzer Pod 2, or leave it unconnected. Use GP Probes or termination adapters to monitor these signals.

** For inverse assembly, only the terminated (2 x 20-pin wide) P4 connector can be used. For timing analysis, use the unterminated 2x10 pin P4 connector.

Configuration File
Use configuration files F68000 or F68010 with the HP E2447AA, or FEC000 with the HP E2447AA for the HP 1670A/D logic analyzer.

To connect to the HP 1671A/D logic analyzer

Use the figure and table below to connect the analysis probe to the HP 1671A/D logic analyzer.



HP 1671A/D	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP E2447AA/AB Connector	not used	not used	P6 *	P1 DATA	P4 ** ADDR/STAT clk ↑	P3 ADDR

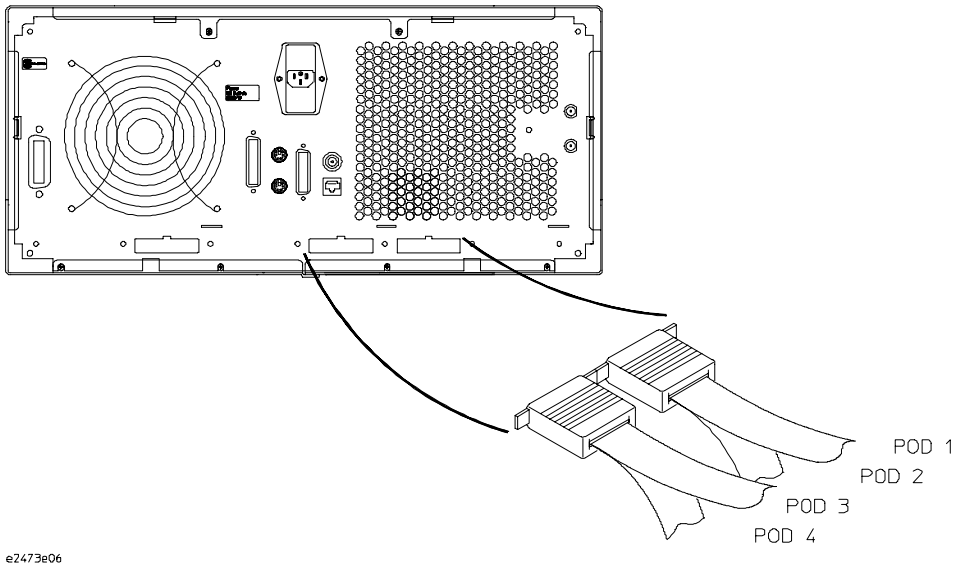
* P6 on the analysis probe is not required for inverse assembly. You can connect it to logic analyzer Pod 2, or leave it unconnected. Use GP Probes or termination adapters to monitor these signals.

** For inverse assembly, only the terminated (2 x 20-pin wide) P4 connector can be used. For timing analysis, use the unterminated 2x10 pin P4 connector.

Configuration File
Use configuration files F68000 or F68010 with the HP E2447AA, or FEC000 with the HP E2447AA for the HP 1671A/D logic analyzer.

To connect to the HP 1672A/D logic analyzer

Use the figure and table below to connect the analysis probe to the HP 1672A/D logic analyzer.

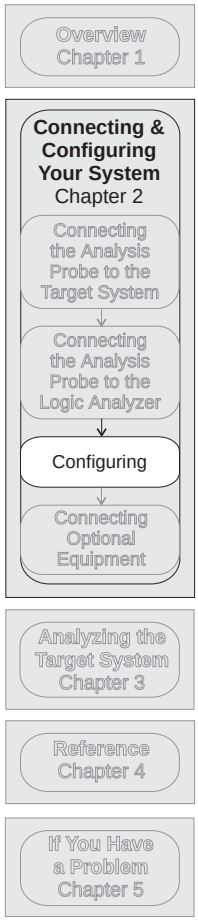


HP 1672A/D	Pod 4	Pod 3	Pod 2	Pod 1
HP E2447AA/AB Connector	P6 *	P1 DATA	P4 ** ADDR/STAT clk ↑	P3 ADDR

* P6 on the analysis probe is not required for inverse assembly. You can connect it to logic analyzer Pod 2, or leave it unconnected. Use GP Probes or termination adapters to monitor these signals.

** For inverse assembly, only the terminated (2 x 20-pin wide) P4 connector can be used. For timing analysis, use the unterminated 2x10 pin P4 connector.

Configuration File
Use configuration files F68000 or F68010 with the HP E2447AA, or FEC000 with the HP E2447AA for the HP 1672A/D logic analyzer.



You configure the logic analyzer by loading a configuration file. The information in the configuration file includes:

- Label names and channel assignments for the logic analyzer
- Inverse assembler file name

The configuration file you use is determined by the logic analyzer you are using. The configuration file names are listed with the logic analyzer connection tables, and in a table at the end of this section.

The procedures for loading a configuration file depend on the type of logic analyzer you are using. There is one procedure for the HP 16600/700 series logic analysis systems, and another procedure for the HP 1660-series, HP 1670-series, and logic analyzer modules in an HP 16500B/C mainframe. Use the appropriate procedures for your analyzer.

To load configuration and inverse assembler files — HP 16600/700 logic analysis systems

If you did not use Setup Assistant, you can load the configuration and inverse assembler files from the logic analysis system hard disk.

1 Click on the File Manager icon. Use File Manager to ensure that the subdirectory /hplogic/configs/hp/m68000/ exists.

> If the above directory does not exist, you need to install the M68000 Processor Support Package. Close File Manager, then use the procedure on the CD-ROM jacket to install the M68000 Processor Support Package before you continue.

2 Using File Manager, select the configuration file you want to load in the /hplogic/configs/hp/m68000/ directory, then click Load. If you have more than one logic analyzer installed in your logic analysis system, use the Target field to select the machine you want to load.

For the E2447AA analysis probe, the appropriate file name ends in "68000" or "68010." For the E2447AB analysis probe, the appropriate file name ends in "EC000."

The logic analyzer is configured for 68000/10 analysis by loading the appropriate configuration file. Loading this file also automatically loads the inverse assembler.

3 Close File Manager.

To load configuration and inverse assembler files — other logic analyzers

If you have an HP 1660-series, HP 1670-series, or logic analyzer modules in an HP 16500B/C mainframe use these procedures to load the configuration file and inverse assembler.

The first time you set up the analysis probe, make a duplicate copy of the master disk. For information on duplicating disks, refer to the reference manual for your logic analyzer.

For logic analyzers that have a hard disk, you might want to create a directory such as 68000 on the hard drive and copy the contents of the floppy onto the hard drive. You can then use the hard drive for loading files.

1. Insert the floppy disk in the front disk drive of the logic analyzer.
2. Go to the Flexible Disk menu.
3. Configure the menu to load.
4. Use the knob to select the appropriate configuration file.

   For the E2447AA analysis probe, the appropriate file name ends in "68000" or "68010." For the E2447AB analysis probe, the appropriate file name ends in "EC000."
5. Select the appropriate analyzer on the menu. The HP 16500 logic analyzer modules are shown in the Logic Analyzer Configuration Files table.
6. Execute the load operation on the menu to load the file into the logic analyzer.

   The logic analyzer is configured for 68000/010 analysis by loading the appropriate configuration file. Loading this file also automatically loads the inverse assembler.

Logic Analyzer Configuration Files

Analyzer Model	Analyzer Description (modules only)	Configuration File
16600A	na	F68000, F68010, or FEC000
16601A	na	F68000, F68010, or FEC000
16602A	na	F68000, F68010, or FEC000
16603A	na	F68000, F68010, or FEC000
16550A (one card)	100 MHz STATE 500 MHz TIMING	F68000, F68010, or FEC000
16554A (one card)	0.5M SAMPLE 70/125 MHz LA	F68000, F68010, or FEC000
16555A (one card)	1.0M SAMPLE 110/250 MHz LA	F68000, F68010, or FEC000
16555D (one card)	2.0M SAMPLE 110/250 MHz LA	F68000, F68010, or FEC000
16556A (one card)	1.0M SAMPLE 100/200 MHz LA	F68000, F68010, or FEC000
16556D (one card)	2.0M SAMPLE 100/200 MHz LA	F68000, F68010, or FEC000
1660A/AS/C/CS/CP	na	F68000, F68010, or FEC000
1661A/AS/C/CS/CP	na	F68000, F68010, or FEC000
1662A/AS/C/CS/CP	na	F68000, F68010, or FEC000
1670A/D	na	F68000, F68010, or FEC000
1671A/D	na	F68000, F68010, or FEC000
1672A/D	na	F68000, F68010, or FEC000

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Chapter 2
Connecting the Analysis Probe to the Target System
Connecting the Analysis Probe to the Logic Analyzer
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Connecting Optional Equipment

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Reference
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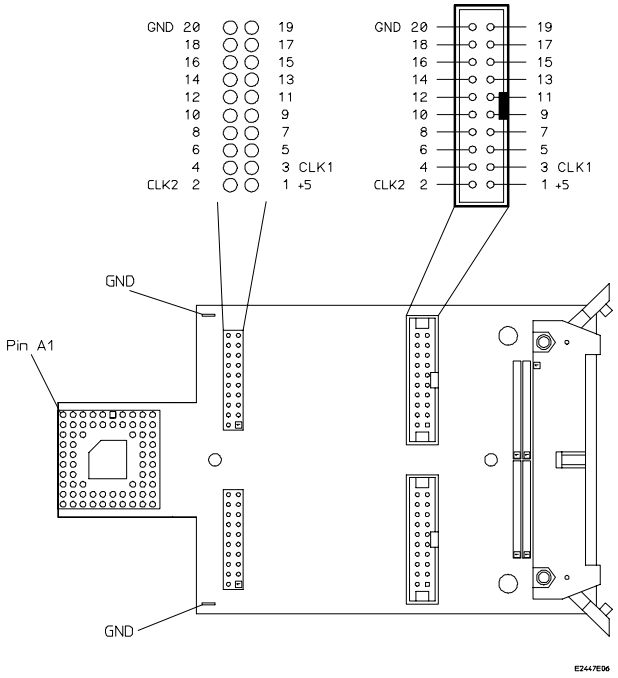
Chapter 5

There is no additional optional equipment supported by the HP E2447AA/AB. You can probe the individual signals with an oscilloscope.

Probing with an oscilloscope

The individual pins on the analysis probe can be probed with an oscilloscope. The figure below shows the top view of the HP E2447AA. There are two ground pins on the top of the analysis probe. Connect the ground lead of the oscilloscope to one of the ground pins on the analysis probe, and the other lead to the signal to be measured. The signals are available on the four non-terminated pods (see top of figure for pin numbers). The signals on the non-terminated pods are the same for the HP E2447AA and the HP E2447AB. The signal-to-pin mapping table in chapter 4 list the correlation between the microprocessor signals, the PGA sockets, and the connectors.

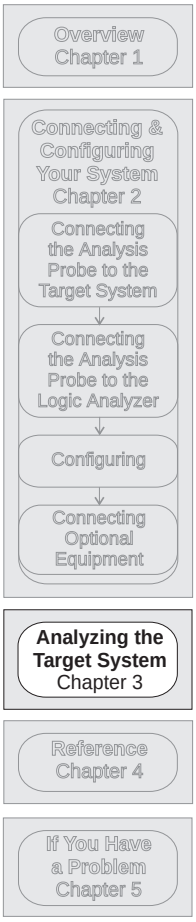


3

Analyzing the Target System

Analyzing the Target System

This chapter describes modes of operation for the HP E2447AA/AB Analysis Probes. It also describes analysis probe data, symbol encodings, and information about the inverse assembler.



The information in this chapter is presented in the following sections:

- Modes of operation
- Logic analyzer configuration
- Using the inverse assembler

Modes of Operation

The HP E2447AA/AB Analysis Probe can be used in two different analysis modes: State-per-transfer and Timing. The following sections describe these operating modes and how to configure the logic analyzer for each mode.

State-per-transfer mode

In State-per-transfer mode, the analysis probe latches A[23:0] and D[15:0] only when there is a valid data transfer. This allows the logic analyzer to capture only valid data when it appears on the bus. The inverse assembly software reconstructs the 68000/010 mnemonic from the raw data. AS clocks the data into the logic analyzer.

Timing mode

The HP E2447AA/AB routes the same signals to both terminated and nonterminated connectors. The terminated connectors have active logic between the microprocessor and the logic analyzer; the nonterminated connectors pass the signals straight through. For Timing analysis, use either General Purpose probes or termination adapters, and connect to Timing connectors P1, P3, and P4. P6 is optional for State and Timing.

The terminated (2x20) P4 connector provides delayed versions of UDS and LDS. For correct Timing analysis of these signals, use the unterminated (2x10) P4, using either a 01650-63203 termination adapter, or the General Purpose probes supplied with your analyzer.

The same format specification loaded for state analysis is also used for timing analysis. To configure the logic analyzer for timing analysis:

1. Select the Configuration menu of the logic analyzer.
2. Select the Type field for the analyzer and select Timing.

   Timing data is displayed in the Waveform menu. Select the Waveform menu, then select the signals which you would like to view. Press run for a new acquisition.

Logic Analyzer Configuration

The following sections describe the logic analyzer configuration as set up by the configuration files.

Trigger specification

The trigger specification is set up by the software to store all states. If you modify the trigger specification to store only selected bus cycles, you may get incorrect or incomplete disassembly.

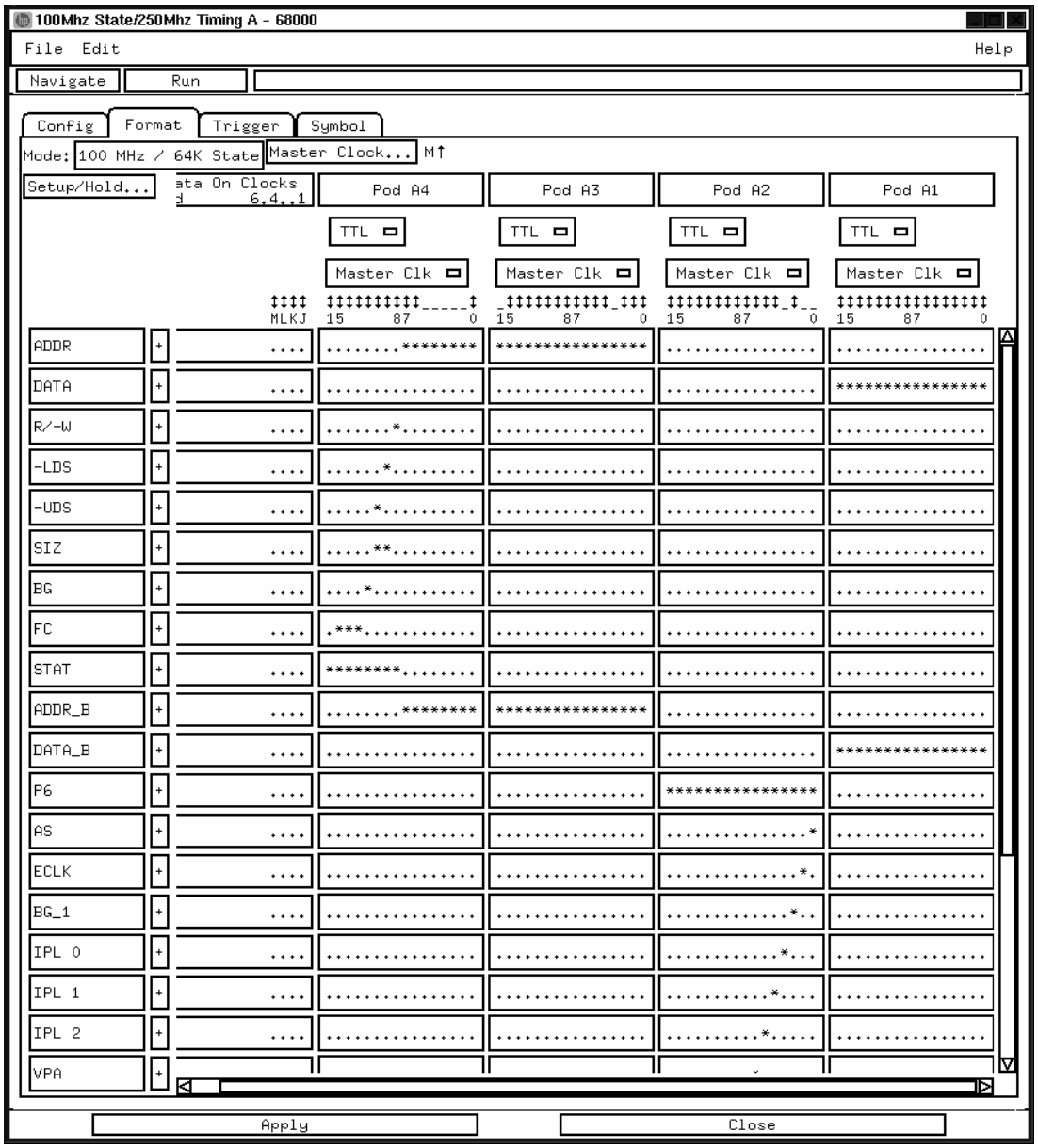
Format specification display

The 68000/010 configuration files contain predefined format specifications. These format specifications include all labels for monitoring the microprocessors.

Chapter 4 of this guide contains a table that lists the signals for the 68000/010 microprocessors and on which pod and probe line the signal comes to the logic analyzer. Refer to this table in chapter 4 and to the logic analyzer connection information for your analyzer in chapter 2 to determine where the signals should be on the format specification screen.

Do not modify the ADDR, DATA, or STAT labels in the format specification if you want inverse assembly. Changes to these labels may cause incorrect or incomplete inverse assembly.

The following screen shows the Format specification display.



Format Listing

Status Encoding

Each of the bits of the STAT label are listed in the table below.

STAT Label Bits

Bit	Status Signals	Description
8	R/W	This signal is high for read cycles and low for write cycles.
9	* LDS	This signal is low when the low byte of the data bus is valid.
10	* UDS	This signal is low when the high byte of the data bus is valid. A combination of the LDS and UDS signals will allow you to determine the size of the data bus transfer.
11	VMA	This signal is low for a Valid Memory Address.
14 - 12	FC0 - FC2	These signals indicate the type of cycle the microprocessor is executing.
clk	AS	

* This is a delayed version of the signal.

Logic Analyzer Symbols

The HP E2447AA/AB configuration software sets up symbol tables on the logic analyzer. The tables contain alphanumeric symbols which identify data patterns or ranges. Labels have been defined in the format specification menu to make triggering on specific cycles easier. The label base in the symbols menu is set to hexadecimal to conserve space in the listing menu.

Select the Symbols field on the format specification menu and then choose a label name from the Label pop-up. The logic analyzer will display the symbols associated with the label.

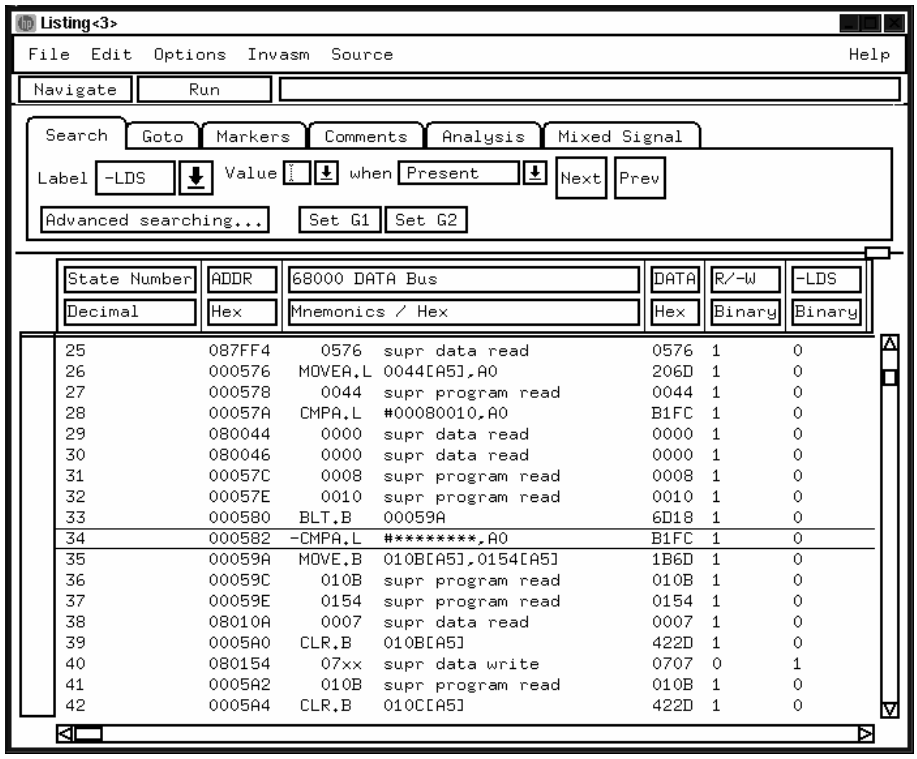
Symbols

Symbol	Pattern
USER DATA WRITE	x001 xxx0
USER DATA READ	x001 xxx1
USER PGRM READ	x010 xxx1
SUPR DATA WRITE	x101 xxx0
SUPR DATA READ	x101 xxx1
SUPR PGRM READ	x110 xxx1
CPU SPACE	x111 xxxx
OPCODE FETCH	xx10 xxx1
SUPR DATA	x101 xxxx
USER DATA	x001 xxxx
DATA	xx01 xxxx
READ	xxxx xxx1
WRITE	xxxx xxx0

The following sections describe the features and output of the inverse assembler.

To display captured state data

Captured data is displayed as shown below. The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly language source code.



State Listing

To align the inverse assembler

The 68000/010 microprocessors do not provide enough status information for the inverse assembler to pick out the first word of an opcode fetch from a series of program reads. To ensure correct disassembly, you must point to a state that contains the first word on an opcode fetch. Once aligned, the inverse assembler will disassemble from this state through the end of the screen.

Use the following procedure to align the inverse assembler:

1. Select a line on the display that you know contains the first state of an instruction fetch.
2. Roll this line to the top of the display.

> Do not roll the instruction to the line number field at the left center screen. In the State Listing, line 25 is the top of the display.

3. Select "Invasm".
4. Select "Align" to align the code.

   The listing inverse assembles from the top line down. Any data before the top of the display is left unchanged.

   Rolling the display up inverse assembles the lines as they appear on the bottom of the display. If you jump to another area of the display by entering a new line number, you may need to re-align the inverse assembler by repeating steps 1 through 4.

   Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

Invasm menu

The HP 16600A/700A logic analysis systems have an Invasm menu in the Listing window. The Invasm menu provides three features: Load, Align, and Options.

Load

The Load function lets you load a different configuration file or inverse assembler. In some cases you may have acquired raw data; you can use the Load function to apply an inverse assembler to that data.

Align

Align enables the inverse assembler to re-align with the microprocessor code. In some cases the prefetch marking algorithm in the inverse assembler may lose synchronization, and unused prefetches or executed instructions may be incorrectly marked.

To align the inverse assembler, use the procedure described earlier.

Options

The Options menu lets you change the width of the display.

Inverse assembler output format

The next few paragraphs describe the general output format of the inverse assembler.

Unused Prefetches (-/?)

The microprocessor may fetch additional instruction words while the last opcode is still being executed. When a program executes an instruction that causes a branch, prefetched words are not used and are discarded by the microprocessor. Unused prefetches are indicated by the prefix "-" in the inverse assembly listing.

The logic analyzer captures prefetches, even if they are not executed. Care must be taken if you are specifying a trigger condition or a storage qualification when the instruction of interest follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microprocessor only prefetches one word, one technique to avoid unwanted triggering from unused prefetches is to add "4" to the trigger address. This trigger condition is only satisfied if the branch is not taken.

In some cases, it is impossible to determine from bus activity whether or not a branch is taken or a prefetch is executed. In these cases, the inverse assembler marks the disassembled line with the prefix "?".

Interpreting Data

The pair of asterisks (**) displayed in the operand field of an instruction indicates that a byte of an expected operand was not stored in the logic analyzer memory. Four asterisks (****) indicate that one word of an expected operand was missing and eight asterisks signify a missing long word. Missing operands (or parts of operands) can result from 68000/68010 instruction prefetch activity or storage qualification.

Examples:

ORI.B	#**,D2	(missing byte operand)
ORI.W	#****,D1	(missing word operand)
ORI.L	#234A****,D3	(missing "lower" word of the operand)
ORI.L	#********,D3	(missing both words of the operand)

In general, asterisks indicate that expected operand fetches are not stored in the logic analyzer memory. Operand fetches may be missed when you add storage qualifications to the standard trace specifications.

The 68000 is capable of supporting byte, word, and long word (32-bit) operands. During operand reads and writes, entire 16-bit (word) values appear on the microprocessor data bus. In the case of single byte operands, the inverse assembler will display "xx" for the byte of the input data that is ignored by the microprocessor. In this manner, it is possible to determine exactly which byte of data the microprocessor has used as an operand.

PC-based Addressing Modes

The 68000 microprocessor may occasionally make an operand fetch from program space when program counter (PC) -based addressing modes are used. For example:

MOVE.L 0[PC,D0.L],D7

When this occurs, the resulting memory read is classified as a program reference by the 68000, and the Function Code lines driven accordingly (they indicate a program read rather than a data read).

When the inverse assembler detects an instruction of this sort, it will attempt to locate the operand fetch and tag it so that it will not be disassembled. Instead, it will be classified as "program data" by the inverse assembler, and displayed in hex.

The table below shows an example. State 350 has the instruction, and states 355 and 356 have the data.

PC-based Addressing Mode Listing

Label Base	> ADDR > Hex		DATA Invasm	STAT Symbol
348	04D214	MOVE.L	D7,FFCE[A4]	USER PGRM READ
349	04D216	FFCE	user program read	USER PGRM READ
350	04D218	MOVE.L	04D654[PC],-[A7]	USER PGRM READ
351	F4083E	43D8	user data write	USER DATA READ
352	F40840	6DFB	user data write	USER DATA READ
353	04D21A	043A	user program read	USER PGRM READ
354	04D21C	MOVE.L	D7,-[A7]	USER PGRM READ
355	04D654	4400	user program data	USER PGRM READ
356	04D656	0000	user program data	USER PGRM READ
357	04D21E	JSR	03523C	USER PGRM READ
358	086BBC	0000	user data write	USER DATA READ
359	086BBA	4400	user data write	USER DATA READ
360	04D220	0003	user program read	USER PGRM READ
361	086BB8	6DFB	user data write	USER DATA READ
362	086BB6	43D8	user data write	USER DATA READ
363	04D222	523C	user program read	USER PGRM READ

Inverse assembler error messages

Any of the following list of error messages may appear during analysis of your target software. Included with each message is a brief explanation.

Data Error Displayed if the trace memory could not be read properly on entry into the inverse assembler.

Illegal Opcode Displayed if the inverse assembler encounters an illegal instruction.

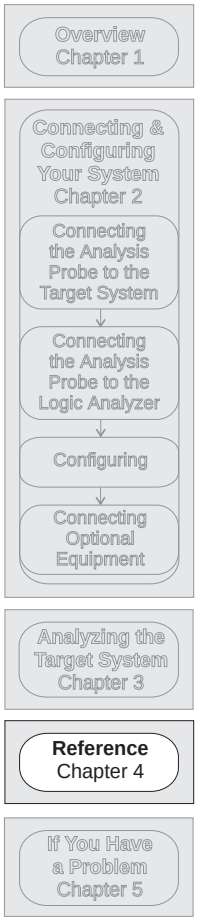
Reference

Reference

This chapter contains additional reference information including the signal mapping for the HP E2447AA/AB Analysis Probe.

The information in this chapter is presented in the following sections:

- Operating characteristics of the analysis probe
- Signal-to-connector mapping
- Circuit board dimensions
- Replaceable parts



Operating characteristics of the analysis probe

The following operating characteristics are not specifications, but are typical operating characteristics for the analysis probe.

Operating Characteristics

Microprocessor Compatibility	Motorola MC68000, MC68010, and MC68HC000 (HP 2447AA), Motorola MC68EC000 (HP E2447AB), and all microprocessors made by other manufacturers that comply with Motorola MC68000/MC68010/MC68HC000, or MC68EC000 specifications.
Microprocessor Package	68-pin PGA (HP E2447AA) 69-pin PLCC (HP E2447AB) PLCC microprocessors must be socketed DIP adapters available from Emulation Technology 68-pin adapter available from Emulation Technology
Accessories Required	None.
Logic Analyzer Required	HP 1660A/AS/C/CS/CP, HP 1661A/AS/C/CS/CP, HP 1662A/AS/C/CS/CP, HP 1670A/D, HP 1671A/D, HP 1672A/D, HP 16550A (one card), HP 16554A/55A/56A (one card), HP 16555D/56D (one card), HP 16600A, HP 16601A, HP 16602A, HP 16603A.
Probes Required	Seven pods of signals are available. Three pods are required for inverse assembly. Three pods are for timing analysis only.
Maximum Clock Speed	16.7 MHz Clock Input.
Power Requirements	100 mA at +5 Vdc maximum from the logic analyzer. CAT I, Pollution degree 2.
Signal Line Loading	100 kOhms plus 18 pF capacitance on all lines except UDS. 50 kOhms plus 30 pF capacitance on UDS.
Microprocessor Operations Displayed	User Data Read/Write User Program Read Supervisor Read/Write Supervisor Program Read Interrupt Acknowledge

Operating Characteristics

Additional Capabilities	The logic analyzer captures all bus cycles, including prefetches.	
Environmental	**This product is intended for indoor use only.**	
Temperature	Operating	0 to 55 degrees C (+32 to +131 degrees F)
	Non-operating	-40 to +75 degrees C (-40 to +167 degrees F)
Altitude	Operating	4,600 m (15,000 ft.)
	Non-operating	15,300 m (50,000 ft.)
Humidity	Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.	

Signal-to-connector mapping

The following table shows the signal-to-connector mapping.

68000/010 Signal List

E2447A Pod / Pin	Logic Analyzer Bit	PGA Pin E2447AA	PLCC Pin E2447AB	68000/68010 Signal	Label
P3 / 19	0	B3	8	* UDS**	ADDR
P3 / 18	1	K4	32	A1	ADDR
P3 / 17	2	J5	33	A2	ADDR
P3 / 16	3	K5	34	A3	ADDR
P3 / 15	4	K6	36	A4	ADDR
P3 / 14	5	J6	37	A5	ADDR
P3 / 13	6	K7	38	A6	ADDR
P3 / 12	7	K8	39	A7	ADDR
P3 / 11	8	J7	40	A8	ADDR
P3 / 10	9	K9	41	A9	ADDR
P3 / 9	10	J8	42	A10	ADDR
P3 / 8	11	J9	43	A11	ADDR
P3 / 7	12	H9	44	A12	ADDR
P3 / 6	13	H8	45	A13	ADDR
P3 / 5	14	J10	46	A14	ADDR
P3 / 4	15	G9	47	A15	ADDR
P3 / 3	CLK	E1	16	CLK	(clock)
P4 / 19	0	H10	48	A16	ADDR
P4 / 18	1	G10	49	A17	ADDR
P4 / 17	2	F9	50	A18	ADDR
P4 / 16	3	F10	51	A19	ADDR
P4 / 15	4	E10	52	A20	ADDR
P4 / 14	5	D10	54	A21	ADDR
P4 / 13	6	C10	55	A22	ADDR
P4 / 12	7	C9	56	A23	ADDR

* This is a delayed version.
** On 68EC000 (E2447AB) this signal is called A0.

68000/010 Signal List (Continued)

E2447A Pod	Logic Analyzer Bit	PGA Pin E2447AA	PLCC Pin E2447AB	68000/68010 Signal	Label
P4 / 11	8	C3	10	R/W	STAT
P4 / 10	9	B2	9	* LDS	STAT
P4 / 9	10	B3	8	* UDS	STAT
P4 / 8	11	G1	12	**VMA (3)	STAT
P4 / 7	12	K3	30	FC0	STAT
P4 / 6	13	J3	29	FC1	STAT
P4 / 5	14	K2	28	FC2	STAT
P4 / 4	15	C1		BGACK (4)	STAT
P4 / 3	CLK	A2	7	AS	(clock)
P1 / 19	0	B4	6	D0	DATA
P1 / 18	1	A3	5	D1	DATA
P1 / 17	2	A4	4	D2	DATA
P1 / 16	3	B5	3	D3	DATA
P1 / 15	4	A5	2	D4	DATA
P1 / 14	5	A6	68	D5	DATA
P1 / 13	6	B6	67	D6	DATA
P1 / 12	7	A7	66	D7	DATA
P1 / 11	8	A8	65	D8	DATA
P1 / 10	9	B7	64	D9	DATA
P1 / 9	10	A9	63	D10	DATA
P1 / 8	11	B8	62	D11	DATA
P1 / 7	12	A10	61	D12	DATA
P1 / 6	13	C8	60	D13	DATA
P1 / 5	14	B9	59	D14	DATA
P1 / 4	15	B10	58	D15	DATA
P1 / 3	CLK	B1	11	DTACK (4)	(clock)

* This is a delayed version.
** This signal is not required to properly clock the logic analyzer. However, it may be useful for other 68000/68010 analysis.
(3) BG on the E2447AB
(4) Not used on the 2447AB

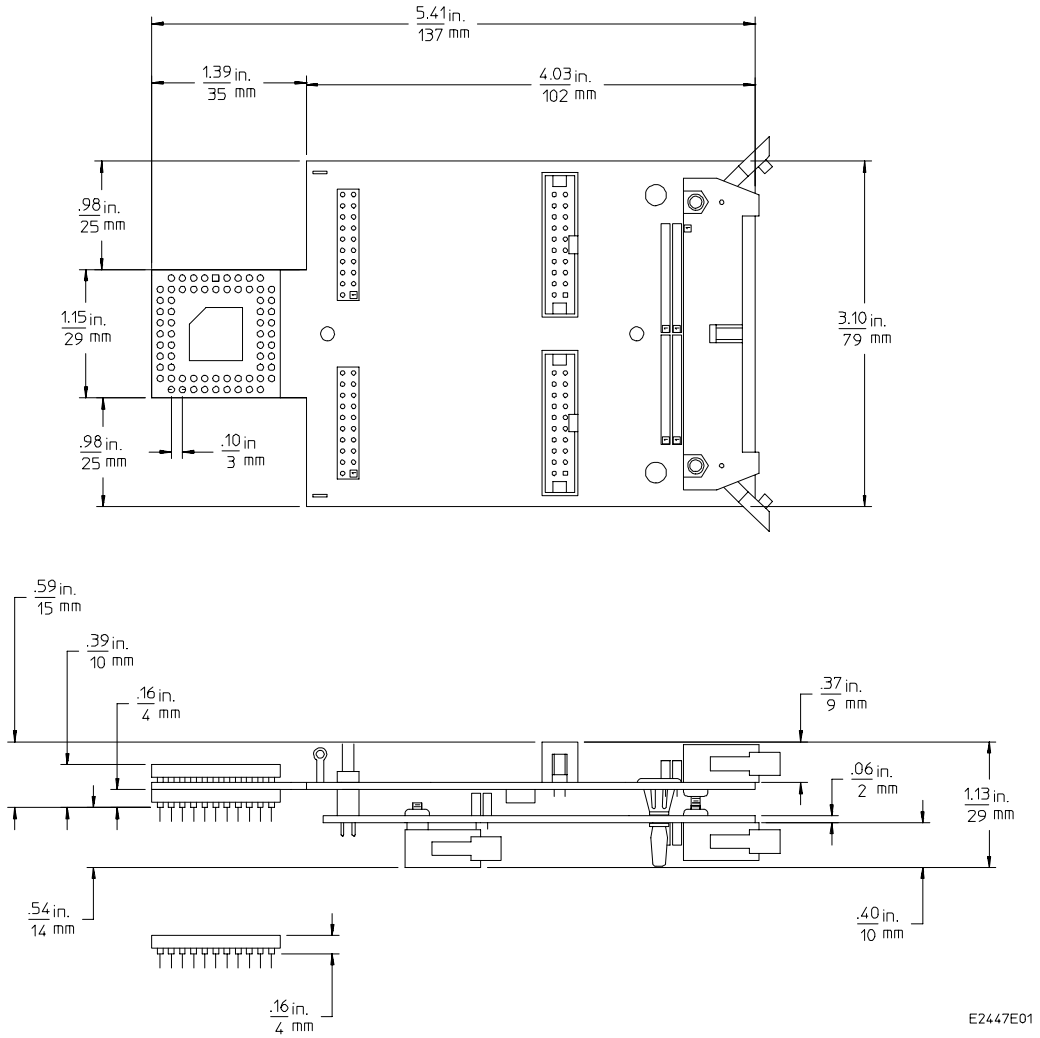
68000/010 Signal List (Continued)

E2447A Pod	Logic Analyzer Bit	PGA Pin E2447AA	PLCC Pin E2447AB	68000/68010 Signal	Label
P6 / 19	0	A2	7	AS	(note 1)
P6 / 18	1	E1	16	ECLK	(note 1,2)
P6 / 17	2	C2	12	BG	(note 1)
P6 / 16	3	J2	27	IPL0	(note 1)
P6 / 15	4	H3	26	IPL1	(note 1)
P6 / 14	5	H2	25	IPL2	(note 1)
P6 / 13	6	G2	--	VPA	(note 1,3)
P6 / 12	7	D1	13	BR	(note 1)
P6 / 11	8	F1	20	HALT	(note 1)
P6 / 10	9	B1	11	DTACK	(note 1)
P6 / 9	10	E1		CLK	(note 1,4)
P6 / 8	11	F2	21	RST	(note 1)
P6 / 7	12	J1	24	BERR	(note 1)
P6 / 6	13		23	AVEC	(note 5)
P6 / 5	14		19	MODE	(note 5)
P6 / 4	15		--	--	

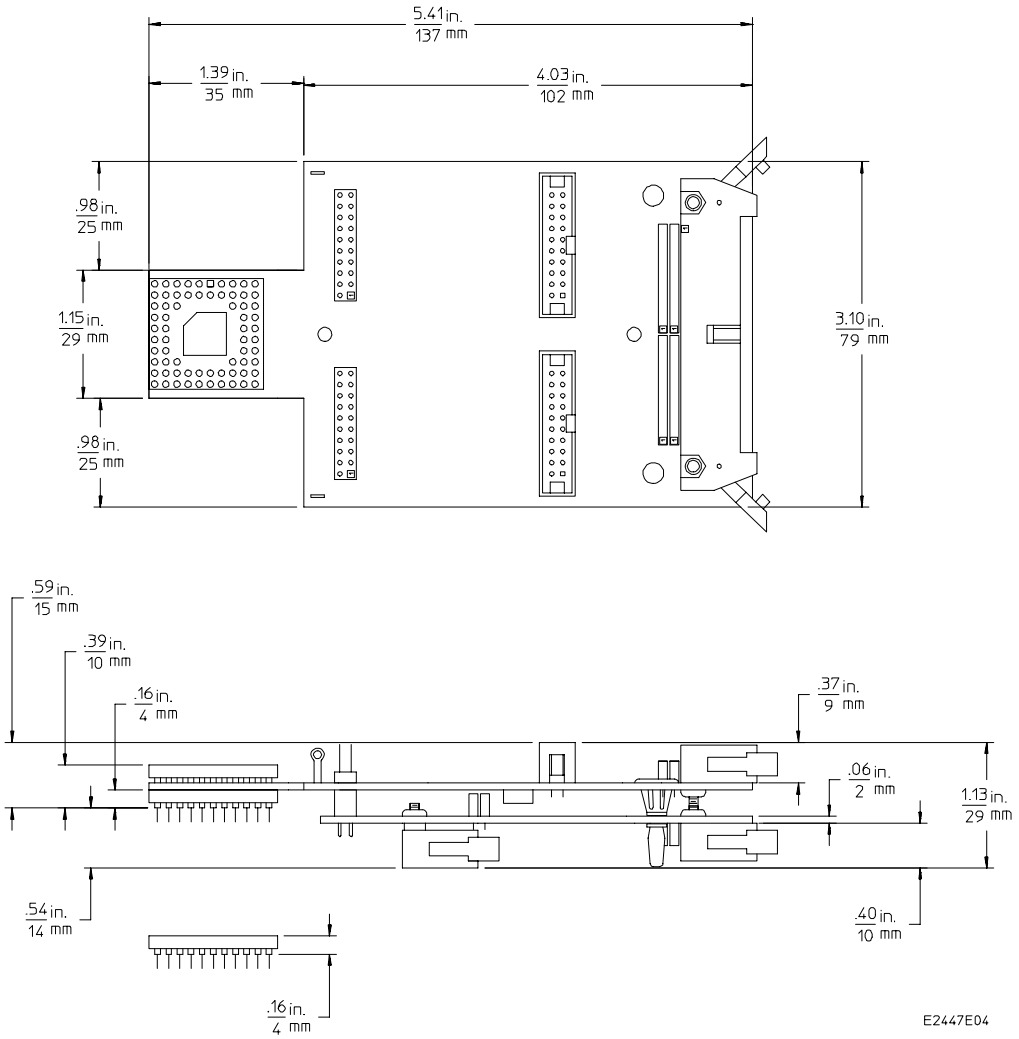
Note 1: These signals are not required for inverse assembly; however, they might be useful for microprocessor analysis.
Note 2 This signal is CLK on the 2447AA.
Note 3: Not used on the 2447AB.
Note 4: Not used on the 2447AB.
Note 5: Not used on the 2447AA.

Circuit board dimensions

The following two figures give the dimensions for the analysis probes. The dimensions are listed in inches and millimeters.



HP E2477AA Circuit Board Dimensions



HP E2477AB Circuit Board Dimensions

Replaceable parts

The repair strategy for this analysis probe is board replacement. However, the table below lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales Office for further information on servicing the board.

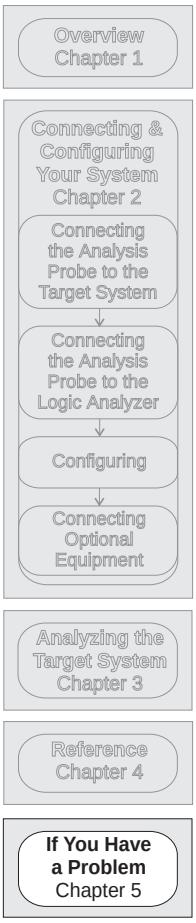
Exchange assemblies are available when a repairable assembly is returned to Hewlett-Packard. These assemblies have been set up on the "Exchange Assembly" program. This lets you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Replaceable Parts

HP Part Number	Description
E2413-66504	Interface Circuit Board
E2447-66501	Personality Circuit Board (E2447AA)
E2447-66502	Personality Circuit Board (E2447AB)
E2434-68701	Inverse Assembler Disk Pouch
1200-1723	69-pin Pin Protector
1200-1721	68-pin Pin Protector, with hole in 69th pin position

If You Have a Problem

If You Have a Problem



Occasionally, a measurement may not give the expected results. If you encounter difficulties while making measurements, use this chapter to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions.

The information in this chapter is presented in the following sections:

- Logic analyzer problems
- Analysis probe problems
- Inverse assembler problems
- Intermodule measurement problems
- Messages
- Cleaning the instrument

If you still have difficulty after trying the suggestions in this chapter, contact your local Hewlett-Packard Service Center.

CAUTION

When you are working with the analyzer, be sure to power down both the analyzer and the target system before disconnecting or connecting cables, probes, and analysis probes. Otherwise, you may damage circuitry in the analyzer, analysis probe, or target system.

Analyzer Problems

This section lists general problems that you might encounter while using the analyzer.

Intermittent data errors

This problem is usually caused by poor connections, incorrect signal levels, or marginal timing.

- ☐ **Remove and reseat all cables and probes, ensuring that there are no bent pins on the analysis probe or poor probe connections.**
- ☐ **Adjust the threshold level of the data pod to match the logic levels in the system under test.**
- ☐ **Use an oscilloscope to check the signal integrity of the data lines.**

  Clock signals for the state analyzer must meet particular pulse shape and timing requirements. Data inputs for the analyzer must meet pulse shape and setup and hold time requirements.

See Also See "Capacitive loading" in this chapter for information on other sources of intermittent data errors.

Unwanted triggers

Unwanted triggers can be caused by instructions that were fetched but not executed.

- ☐ **Add the prefetch queue or pipeline depth to the trigger address to avoid this problem.**

  The logic analyzer captures prefetches, even if they are not executed. When you are specifying a trigger condition or a storage qualification that follows an instruction that may cause branching, an unused prefetch may generate an unwanted trigger.

No activity on activity indicators

- ☐ Check for loose cables, board connections, and analysis probe connections.
- ☐ Check for bent or damaged pins on the analysis probe.

No trace list display

If there is no trace list display, it may be that your trigger specification is not correct for the data you want to capture, or that the trace memory is only partially filled.

- ☐ Check your trigger sequencer specification to ensure that it will capture the events of interest.
- ☐ Try stopping the analyzer; if the trace list is partially filled, this should display the contents of trace memory.

Analyzer won't power up

If the logic analyzer power is powered down when it is connected to a powered-up target system, the logic analyzer may not be able to power up. Some logic analyzers are inhibited from powering up when they are connected to a target system that is already powered up.

- ☐ Disconnect all logic analyzer cabling from the analysis probe. This will allow the logic analyzer to power up. Reconnect logic analyzer cabling after power up.

Analysis Probe Problems

This section lists problems that you might encounter when using an analysis probe. If the solutions suggested here do not correct the problem, you may have a damaged analysis probe. Contact your local Hewlett-Packard Sales Office if you need further assistance.

Target system will not boot up

If the target system will not boot up after connecting the analysis probe, the microprocessor (if socketed) or the analysis probe may not be installed properly, or they may not be making electrical contact.

- ☐ **Ensure that you are following the correct power-on sequence for the analysis probe and target system.**

  1 Power up the analyzer and analysis probe.

  2 Power up the target system.

  If you power up the target system before you power up the analysis probe, interface circuitry in the analysis probe may latch up and prevent proper target system operation.

- ☐ **Verify that the microprocessor and the analysis probe are properly rotated and aligned so that the index pin on the microprocessor (pin 1 or pin A1) matches the index pin on the analysis probe.**

- ☐ **Verify that the microprocessor and the analysis probe are securely inserted into their respective sockets.**

- ☐ **Verify that the logic analyzer cables are in the proper sockets of the analysis probe and are firmly inserted.**

Erratic trace measurements

There are several general problems that can cause erratic variations in trace lists and inverse assembly failures.

- ☐ **Do a full reset of the target system before beginning the measurement.**

  Some analysis probe designs require a full reset to ensure correct configuration.

- ☐ **Ensure that your target system meets the timing requirements of the processor with the analysis probe installed.**

  See “Capacitive Loading” in this chapter. While analysis probe loading is slight, pin protectors, extenders, and adapters may increase it to unacceptable levels. If the target system design has close timing margins, such loading may cause incorrect processor functioning and give erratic trace results.

- ☐ **Ensure that you have sufficient cooling for the microprocessor.**

  Some microprocessors generate substantial heat. This is exacerbated by the active circuitry on the analysis probe board. You should ensure that you have ambient temperature conditions and airflow that meet or exceed the requirements of the microprocessor manufacturer.

Capacitive loading

Excessive capacitive loading can degrade signals, resulting in incorrect capture by the analysis probe, or system lockup in the microprocessor. All analysis probes add additional capacitive loading, as can custom probe fixtures you design for your application.

Careful layout of your target system can minimize loading problems and result in better margins for your design. This is especially important for systems that are running at frequencies greater than 50 MHz.

- ☐ **Remove as many pin protectors, extenders, and adapters as possible.**

- ☐ **If multiple analysis probe solutions are available, use one with lower capacitive loading.**

Inverse Assembler Problems

This section lists problems that you might encounter while using the inverse assembler.

When you obtain incorrect inverse assembly results, it may be unclear whether the problem is in the analysis probe or in your target system. If you follow the suggestions in this section to ensure that you are using the analysis probe and inverse assembler correctly, you can proceed with confidence in debugging your target system.

No inverse assembly or incorrect inverse assembly

This problem may be due to incorrect alignment, modified configuration files, incorrect connections, or a hardware problem in the target system. A locked status line can cause incorrect or incomplete inverse assembly.

- ☐ **Ensure that each logic analyzer pod is connected to the correct analysis probe connector.**

  There is not always a one-to-one correspondence between analyzer pod numbers and analysis probe cable numbers. Microprocessor interfaces must supply address (ADDR), data (DATA), and status (STAT) information to the analyzer in a predefined order. The cable connections for each analysis probe are often altered to support that need. Thus, one analysis probe might require that you connect cable 2 to analyzer pod 2, while another will require you to connect cable 5 to analyzer pod 2. See Chapter 2 for connection information.

- ☐ **Check the activity indicators for status lines locked in a high or low state.**

- ☐ **Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values.**

  These labels must remain as they are configured by the configuration file. Do not change the names of these labels or the bit assignments within the labels. Some analysis probes also require other data labels. See Chapter 3 for more information.

- ☐ **Verify that all microprocessor caches and memory managers have been disabled.**

  In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly. It may be incorrect because a portion of the execution trace was not visible to the logic analyzer.

- ☐ **Verify that storage qualification has not excluded storage of all the needed opcodes and operands.**

Inverse assembler will not load or run

You need to ensure that you have the correct system software loaded on your analyzer.

- ☐ **For the HP 16600/700 logic analysis systems, the inverse assembler must be installed on the hard drive using the procedures listed on the jacket for the CD ROM. Re-install the Processor Support Package for this product, then try loading the configuration file again.**

- ☐ **For other logic analyzers, ensure that the inverse assembler is on the same disk as the configuration files you are loading.**

  Configuration files for the state analyzer contain a pointer to the name of the corresponding inverse assembler. If you delete the inverse assembler, rename it, or use the File Manager Copy command to copy it to the HP 16600/700 logic analysis systems, the configuration process will fail to load the inverse assembler.

  See Chapter 3 for details.

Intermodule Measurement Problems

Some problems occur only when you are trying to make a measurement involving multiple modules.

An event wasn't captured by one of the modules

If you are trying to capture an event that occurs very shortly after the event that arms one of the measurement modules, it may be missed due to internal analyzer delays. For example, suppose you set the oscilloscope to trigger upon receiving a trigger signal from the logic analyzer because you are trying to capture a pulse that occurs right after the analyzer's trigger state. If the pulse occurs too soon after the analyzer's trigger state, the oscilloscope will miss the pulse.

- **Adjust the skew in the Intermodule menu.**

  You may be able to specify a skew value that enables the event to be captured.

- **Change the trigger specification for modules upstream of the one with the problem.**

  If you are using a logic analyzer to trigger the scope, try specifying a trigger condition one state before the one you are using. This may be more difficult than working with the skew because the prior state may occur more often and may not always be related to the event you are trying to capture with the oscilloscope.

Analyzer Messages

This section lists some of the messages that the analyzer displays when it encounters a problem.

". . . Enhanced Inverse Assembler Not Found"

This error only occurs on the HP 16600/700 logic analysis systems. This error occurs if you rename or delete the enhanced inverse assembler file that is attached to the configuration file, or if you do not properly install the inverse assembler file on the hard disk. Ensure that the inverse assembler file is not renamed or deleted. If you use the File Manager Copy command to copy an inverse assembler to the HP 16600/700 logic analysis systems, the enhanced inverse assembler will not load. Use the Install procedures listed on the jacket of the CD ROM to install the files for this product.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

For the HP 16600/700 logic analysis systems, the inverse assembler must be installed on the hard drive using the procedures listed on the jacket for the CD ROM.

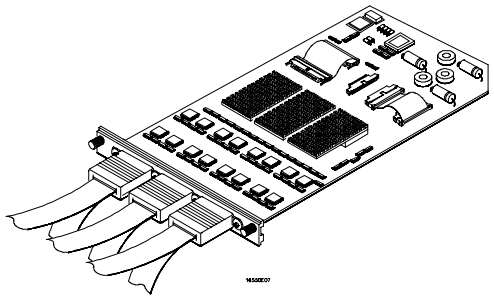
For other logic analyzers, if you have copied the files to the logic analyzer hard disk, ensure that the inverse assembler is located in the same directory as the configuration file.

". . . Does Not Appear to be an Inverse Assembler File"

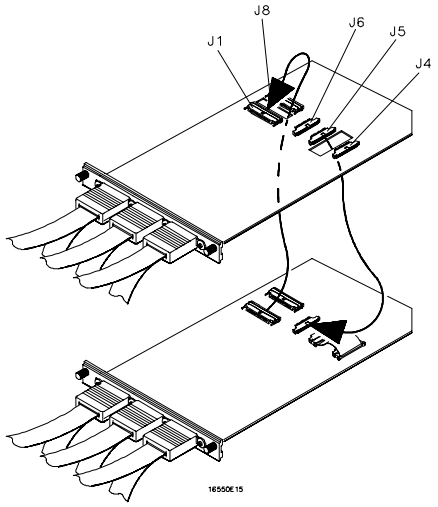
This error occurs if the inverse assembler file requested by the configuration file is not a valid inverse assembler. Use the Install procedures listed on the jacket of the CD ROM to re-install the files for this product.

"Measurement Initialization Error"

This error occurs when you have installed the cables incorrectly on logic analysis cards. The following diagrams show the correct cable connections for one-card and two-card HP 16550A installations. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.



Cable Connections for One-Card HP 16550A Installations

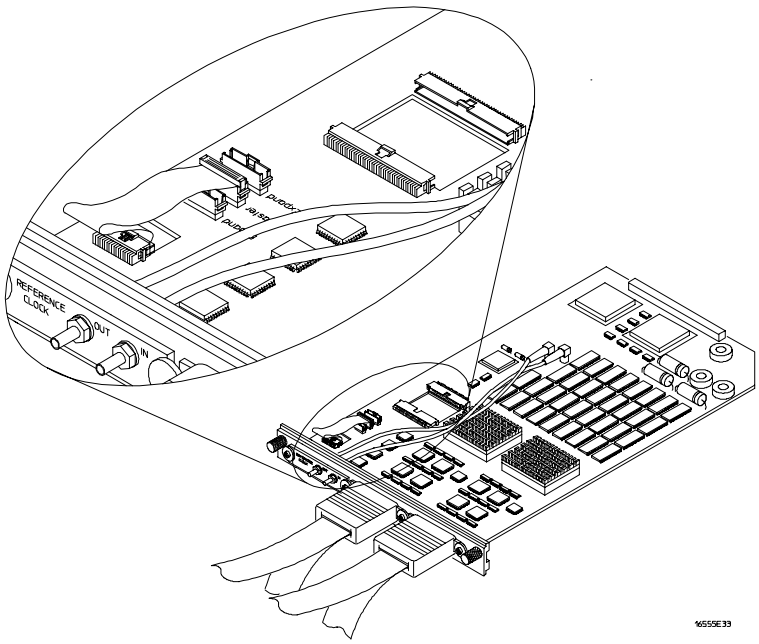


Cable Connections for Two-Card HP 16550A Installations

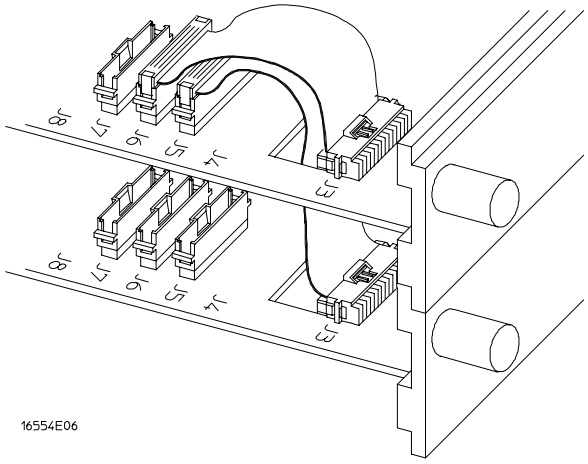
See Also

The *HP 16550A 100-MHz State/500-MHz Timing Logic Analyzer Service Guide*.

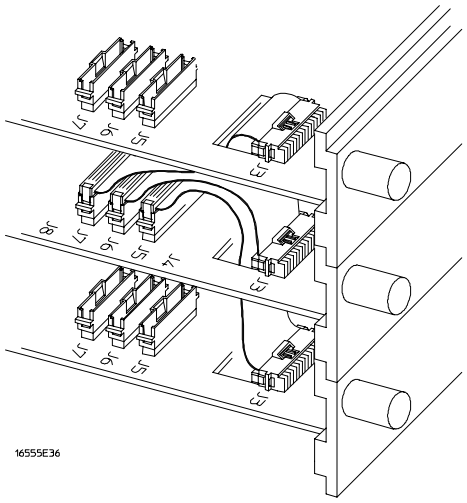
The following diagrams show the correct cable connections for one-card, two-card, and three-card installations on HP 16554A, HP 16555A/D, and HP 16556A/D logic analysis cards. Ensure that your cable connections match the silk screening on the card, and that they are fully seated in the connectors. Then, repeat the measurement.



Cable Connections for One-Card HP 16554/55/56 Installations



Cable Connections for Two-Card HP 16554/55/56 Installations



Cable Connections for Three-Card HP 16554/55/56 Installations

See Also

The HP 16554A 70-MHz State/250-MHz Timing Logic Analyzer Service Guide.

The HP 16555A 110-MHz State/250-MHz Timing Logic Analyzer Service Guide.

The HP 16556A 100-MHz State/400-MHz Timing Logic Analyzer Service Guide.

"No Configuration File Loaded"

This is usually caused by trying to load a configuration file for one type of module/system into a different type of module/system.

- ☐ Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500A/B/C disk operation menu. Selecting Load {All} will cause incorrect operation when loading most analysis probe configuration files.

See Also Chapter 2 describes how to load configuration files.

"Selected File is Incompatible"

This occurs when you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

"Slow or Missing Clock"

- ☐ This error message might occur if the logic analyzer cards are not firmly seated in the logic analysis system mainframe. Ensure that the cards are firmly seated.
- ☐ This error might occur if the target system is not running properly. Ensure that the target system is on and operating properly.
- ☐ If the error message persists, check that the logic analyzer pods are connected to the proper connectors on the analysis probe. See Chapter 2 to determine the proper connections.

“Time from Arm Greater Than 41.93 ms”

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

“Waiting for Trigger”

If a trigger pattern is specified, this message indicates that the specified trigger pattern has not occurred. Verify that the triggering pattern is correctly set.

- When analyzing microprocessors that fetch only from word-aligned addresses, if the trigger condition is set to look for an opcode fetch at an address not corresponding to a word boundary, the trigger will never be found.

Cleaning the Instrument

If this instrument requires cleaning, disconnect it from all power sources and clean it with a mild detergent and water. Make sure the instrument is completely dry before reconnecting it to a power source.

Glossary

Analysis Probe A probe connected to the target microprocessor. It provides an interface between the signals of the target microprocessor and the inputs of the logic analyzer.

Connector Board A board whose only function is to provide connections from one location to another. One or more connector boards might be stacked to raise a probe above a target micoprocessor to avoid mechanical contact with other components installed close to the target microprocessor.

Elastomeric Probe Adapter A connector that is fastened on top of a target microprocessor using a retainer and knurled nut. The conductive elastomer on the bottom of the probe adapter makes contact with pins of the target microprocessor and delivers their signals to connection points on top of the probe adapter.

Emulation Module An emulation module is installed within the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Probe.

Emulation Probe An emulation probe is a stand-alone instrument connected to the mainframe of a logic analyzer. It provides run control within an emulation and analysis test setup. See Emulation Module.

Flexible Adapter Two connection devices coupled with a flexible cable. Used for connecting probing hardware on the target microprocessor to the analysis probe.

General-purpose Flexible Adapter A cable assembly that connects the signals from an elastomeric probe adapter to an analysis probe. Normally, a male-to-male header or transition board makes the connections from the general-purpose flexible adapter to the analysis probe.

High-Density Adapter Cable A cable assembly that delivers signals from an analysis probe hardware interface to the logic analyzer pod cables. A high-density adapter cable has a single Mictor connector that is installed into the analysis probe, and two cables that are connected to corresponding odd and even logic analyzer pod cables.

High Density Termination Adapter Cable Same as a High Density Adapter Cable, except it has a termination in the Mictor connector.

Jumper Moveable direct electrical connection between two points.

Mainframe Logic Analyzer A logic analyzer that resides on one or more board assemblies installed in an HP 16500B/C, 1660xA, or 16700A mainframe.

Male-to-male Header A board assembly that makes point-to-point connections between the female pins of a flexible adapter or transition board and the female pins of an analysis probe.

Preprocessor Interface See Analysis Probe.

Preprocessor Probe See Analysis Probe.

Probe adapter See Elastomeric Probe Adapter.

Processor Probe See Emulation Probe and Emulation Module.

Prototype Analyzer The HP 16505A prototype analyzer acts as an analysis and display processor for the HP 16500B/C logic analysis system. It provides a windowed interface and powerful analysis capabilities.

Setup Assistant A software program that guides you through the process of connecting and configuring an analysis probe and logic analyzer to make measurements on a specific microprocessor.

Shunt Connector. See Jumper.

Stand-alone Logic Analyzer A stand-alone logic analyzer has a predefined set of hardware components which provide a specific set of capabilities. It is designed to perform logic analysis. A stand-alone logic analyzer differs from a mainframe logic analyzer in that it does not offer card slots for installation of additional capabilities, and its specifications are not modified based upon selection from a set of optional hardware boards that might be installed within its frame.

Transition Board A board assembly that obtains signals connected to one side and re-arranges them in a different order for delivery at the other side of the board.

1/4-Flexible Adapter An adapter that obtains one-quarter of the signals from an elastomeric probe adapter (one side of a target microprocessor) and makes them available for probing.

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New editions are complete revisions of the manual. Many product updates do not require manual changes; and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.